MICRO AND NANOFABRICATION FOR OPTOMECHANICS

Cavity Quantum Optomechanics

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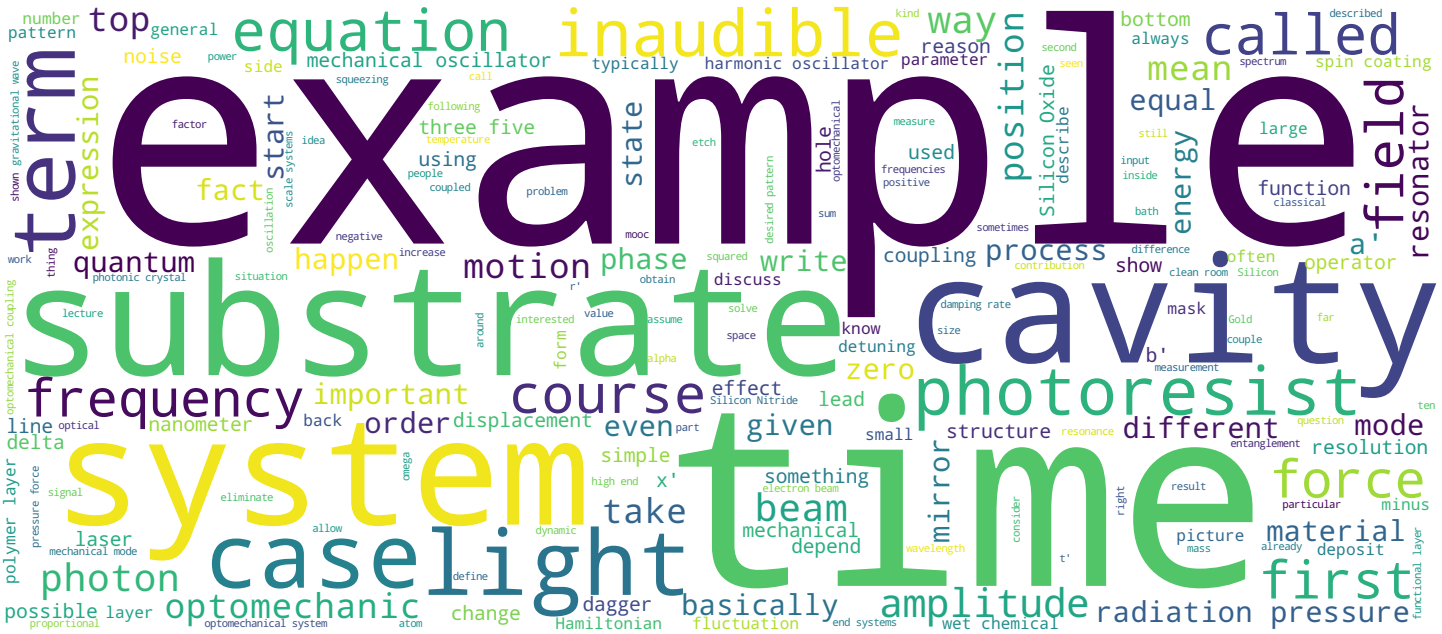
GHENT UNIVERSITY



Search MOOC

Video

EPFL

MICRO- AND NANOFABRICATION IS KEY

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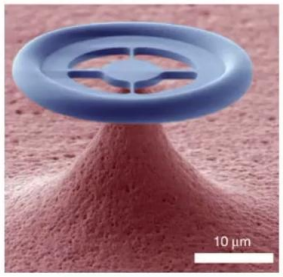
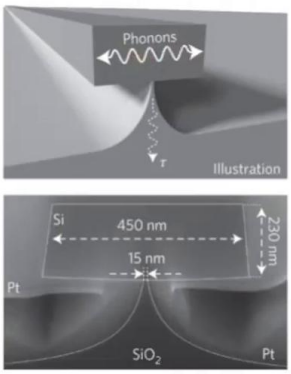
Ultra-high Q SiO_2 toroid resonator



E Verhagen *et al. Nature* **482**, 63-67 (2012)
doi:10.1038/nature10787

SBS in silicon waveguides



R. Van Laer *et al. Nature Phot.* 9, 199-203 (2015)
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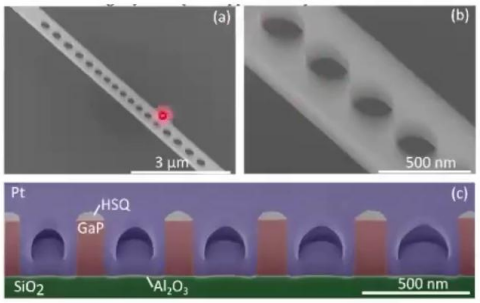
Gallium Phosphide Photonc Crystal Cavities



K. Schneider *et al.* ***Optica*** 6, 577-584 (2019)
doi: 10.1364/OPTICA.6.000577

My name is Dries Van Thourhout and I'm a Professor at Ghent University. In this session of the mooc, I will talk about micro and nanofabrication techniques for optomechanics. The reason I want to do that is obvious. If you look at the recent literature then you will see that many breakthroughs in the field of optomechanics actually very heavily rely on very advanced micro and nanofabrication techniques. This is classic example of the ultra-high Q Silicon Oxide toroid resonator which was the basis of many seminal experiments in the field. Another example from our own work is the Silicon waveguide which is enriched in such a way that it rests just on a very thin pillar of Silicon Oxide. This allows the structure to move sideways and allowed us to demonstrate for the first time stimulated Brillouin scattering in Silicon waveguides. Another example here from IBM in Zurich is this gallium phosphide photonic crystal cavity. Gallium phosphide is a very interesting material because it shows a high electro-optic and a high piezoelectric effect and is also less susceptible to so-called two-photon absorption compared to, for example, Silicon.

Notes

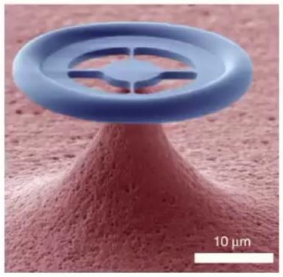
Summary

0m 00s

MICRO- AND NANOFABRICATION IS KEY

Many recent breakthroughs in the field of optomechanics rely on very advanced micro- and nanofabrication

Ultra-high Q SiO_2 toroid resonator



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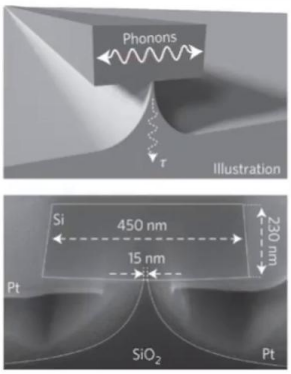

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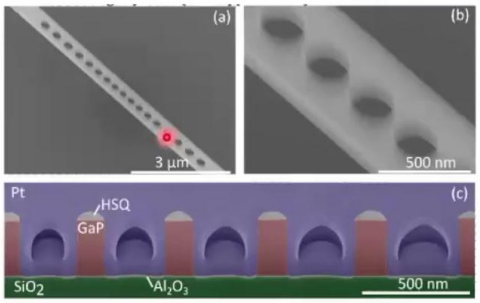

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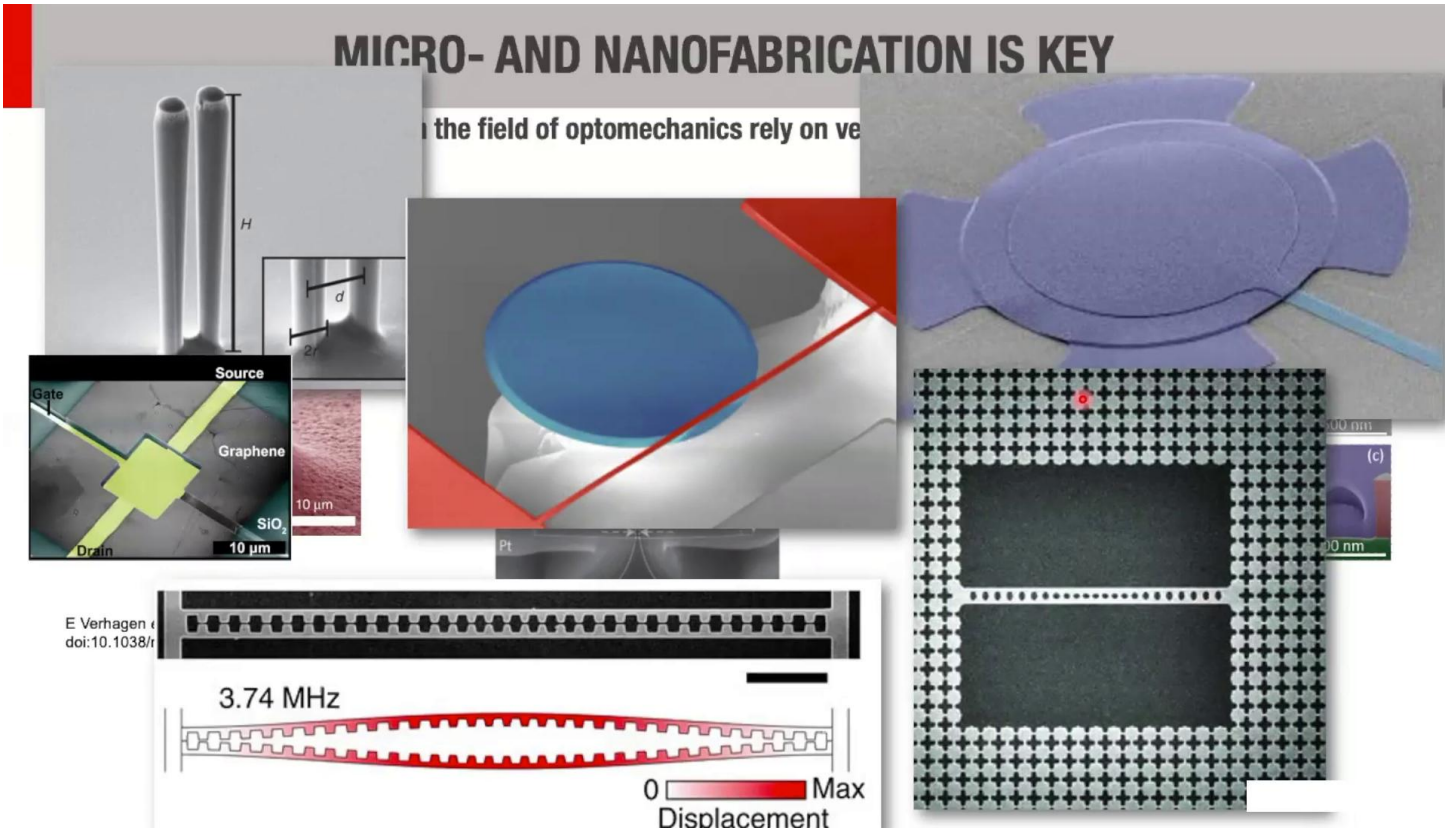
I included this example to show you're not only interested in the classic materials like Silicon, Silicon Oxide, Glass but also might be interested in more novel materials like these single conductor *[inaudible]* lightweight material and so on.

Notes

Summary

1m 08s



And there are, of course, many many more examples where this is all relevant.

Notes

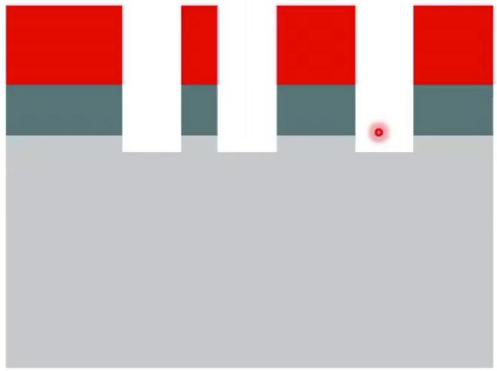
Summary

1m 21s

OUTLINE: GENERAL FABRICATION FLOW

Most important processing steps:

- A suitable substrate
- Deposition of functional layer(s)
- Lithography
- Etch functional layer



So how does a general fabrication flow looks like? I will give a very simplified overview here and the starting point, of course, is the substrates. In many cases that will be Silicon but it could also be glass or three-five semiconductor or basically anything which is flat. On top of that you then deposit your functional layer. In this example, for example, Silicon Nitride layer would also be again a semiconductor layer or a metal or wire. Next you want to pattern this layer. And the way the process we use for that is so-called lithography process. Starts with spin coating a photosensitive polymer layer that photoresist and then we eliminate that layer through a mask which contains the desired pattern such that the photoresist is exposed and becomes soluble at least the exposed patterns become soluble in a developer afterwards. Then we have the pattern in a photoresist and we just have to transfer it in functional layer, for example, using a wet chemical etching process. Finally, we of course, want to remove this photoresist layer *[inaudible]*.

Notes

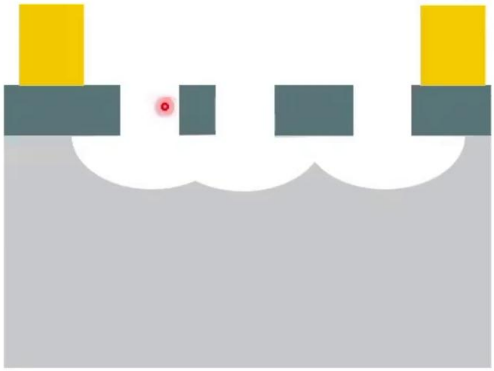
Summary

1m 28s

OUTLINE: GENERAL FABRICATION FLOW

Most important processing steps:

- Deposition of suitable layer(s)
- Lithography
- Etching
- Metallisation
- Release



We could repeat this process over and over. For example, we also may want to deposit a metal layer on top of that. And, of course, here we have the same sequence of using a photoresist to pattern the layer and so. Finally, we maybe as we are in the domain of optomechanics we want to release some of the searches and with releasing I mean we want to make them free from a substrate such that we can move them around, for example, by applying electrical field we can move them here. So this release process is very typical for optomechanics or for MEMS, Micro Electromechanical Structures, in general. And I will discuss it also in the course of this session.

Notes

Summary

2m 37s

LITHOGRAPHY

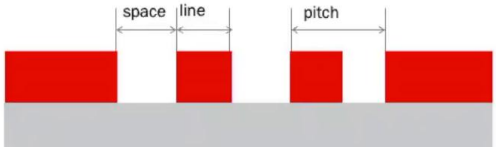
Define the desired pattern in a photo-sensitive polymer layer

Two main approaches:

- Mask-based lithography: write the full pattern at once by projecting a prefabricated mask on the photo-sensitive polymer layer ⟹ photo-resist
- Direct-write lithography: write the desired pattern pixel-by-pixel using a focused electron or laser beam. ⟹ ebeam-resist

Resolution (CD - critical dimension): smallest line/space that can be defined with given approach

- from few nanometer (electron beam) to few micrometer (low end lab mask aligner)



So this is the outline of the session. Basically in this mooc, we will cover all the processes that I just talked about. Lithography, layer deposition, etching, layer release, bonding and planarization and then some concluding remarks. First, lithography. First and probably also the most important process. So the idea is that you define a desired pattern in a photosensitive polymer layer. There are two main classes of lithography processes and there are so called mask-based lithography processes whereby you write the full pattern at once by projecting a prefabricated mask on a photosensitive polymer layer and there are the direct-write lithography processes where you write a desired pattern pixel by pixel using, in most cases, focused electron beam but it could also be a focused laser beam. In the first case, you use a photoresist and in second phase an e-beam resist. Important parameters in these processes are the resolution or so-called CD or Critical Dimension. It's basically the smallest line or space that you can define with a given approach and so with line and space we mean for example, the *[inaudible]* photoresist here and then the space is a opening between two photoresists.

Notes

Summary

3m 20s

LITHOGRAPHY

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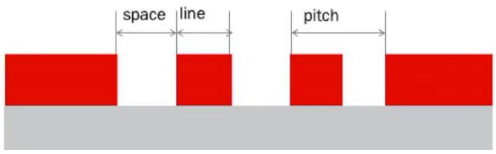
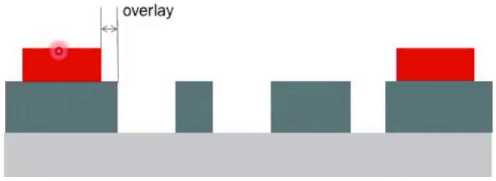
- from few nanometer (electron beam) to few micrometer (low end lab mask aligner)

Alignment accuracy

- Good alignment accuracy (overlay) is critical when carrying out multiple process steps on same substrate
- From few nanometer to few micrometer





Actually more relevant is actually the pitch if you have a periodic pattern. The pitch is actually what ultimately will determine the resolution. The reason I'm saying that is that if you just have to define a line in, for example, a very wide and have very wide spaces, you can also make the always make the lines as narrow as you want by, for example, over-developing using over development and where you cut the line from the sides and you can make it as narrow as you want. But if you really want a periodic pattern with a certain pitch then you're fundamentally limited by diffraction *[inaudible]*. You're familiar with your background in optics. So these critical dimensions can be a few micrometers from mask-based low and to mask-based aligners to a few nanometers for electron mean processes. Another important parameter is so-called alignment accuracy or overlay so if you want to deposit multiple of these layers on top of each other, of course, you want them to be aligned with respect to each other. It's also very critical. Let me again from a few nanometer for high-end systems to a few micrometers for the low-end systems.

Notes

Summary

4m 31s

ELECTRON BEAM LITHOGRAPHY

Use high-energy electron beam to write desired pattern in polymer layer

- Beam is scanned over surface, typically in raster scan
- With sufficient dose (Coulomb/cm^2) resist becomes soluble/insoluble in suitable developer (positive/negative resist)

Lab-scale systems (1-30KeV)
("converted SEM")

Industrial scale systems (up to 100KeV)
("designed for high throughput and fully automated operation")

Let's first have a look at electron beam lithography. So the idea is very simple. You use a high-energy electron beam to write a desired pattern in the polymer layer. And the beam is scanned over the surface typically in the raster scan. We have more complex systems but it's not so relevant now here. And then with sufficient dose, the resistance will become soluble or insoluble in a suitable developer and then we're talking about the positive photoresist and negative photoresist. Then I have very large industrial scale systems with accelerations for the electrons up to one hundred kilo electron volts which is sometimes available in high-end clean rooms also in university scale but in most cases university scale you use the smaller-end systems with an acceleration up to 30 kilo electron volts. Basically these are converted as the end-systems all these high-end systems are really purposely built for these vacuum. The advantage of the higher acceleration voltage is simply higher resolution and also less so-called proximity effects. I'll come back to that in a minute. But the disadvantage is a high cost of the system both from purchase and maintenance.

Notes

Summary

5m 40s

ELECTRON BEAM LITHOGRAPHY

Lab-scale systems (1-30KeV)
("converted SEM")

Use high-energy electron beam to write desired pattern in polymer layer

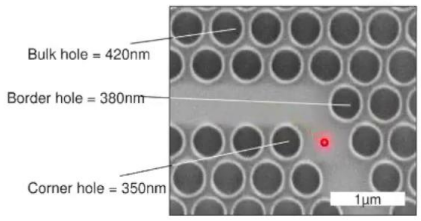
- Beam is scanned over surface, typically in raster scan
- With sufficient dose (Coulomb/cm^2) resist becomes soluble/insoluble in suitable developer (positive/negative resist)

High Resolution Possible

- From 50 nm down to few nm
- Depends on beam quality, photoresist (thickness, type...), developmer

Challenges:

- Stitching
- Proximity effects, overlay...



Industrial scale systems (up to 100KeV)
("designed for high throughput and fully automated operation")

These and all other systems allow for high resolution from 15 nanometer down to a few nanometer. And that depends on the beam quality. Even for these low-end lab systems the beam quality the beam is often smaller than a few nanometer. But the problem is that this beam will deflect in your photoresist and the substrate and then form a larger pattern basically that will then determine your resolution. For the very high-end processes where you want to reach ultimate resolution also the photoresist itself and then the the length of the polymer chains the inlet photoresist might play a role. So then that might become extremely relevant. Challenges are stitching so these patterns are typically written in so-called fields which are not that large, can be a few tens of micrometer to maybe 500 micrometer. These fields have then to be connected to each other if you want to write higher patterns larger patterns and also proximity effects might be important in an example which you see here in the bottom so here we try to write a waveguide in a 2D photonic crystal. At first sight everything looks well and you see nicely defined holes.

Notes

Summary

6m 52s

ELECTRON BEAM LITHOGRAPHY

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("converted SEM")

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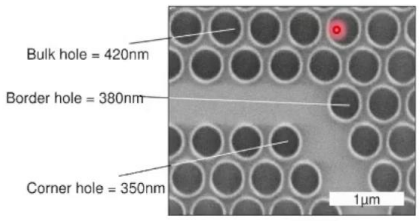


But then if you look more accurately and start to measure these holes then you'll see that the holes in the bulk are quite a bit larger than the ones at the sides and there's even an effect here at the corner holes. The reason is that in the bulk so these holes also do not only see the directly the electrons directly incident over here but also some of the electrons which are incident over here are backscattered through the substrate over here and will result so in a higher local dose and so in larger dimensions. So these effects can be taken into account. In simulation, you have special simulation packages to take that into account that it's far from here.

Notes

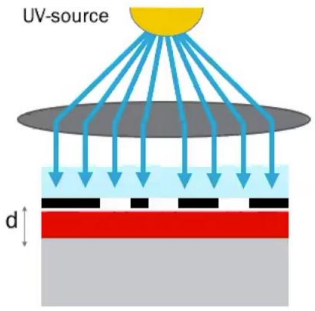
Summary

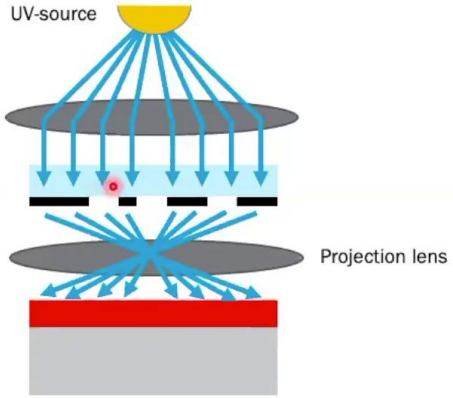
8m 12s

OPTICAL LITHOGRAPHY

UV-light illuminates photoresist through suitable mask ⟹ Typically chrome on glass

Two main classes of lithography systems: contact/proximity aligner and projection aligner





- Mask in direct contact with substrate
- "Simple"
- Lab-scale systems
- Resolution: $\sim\sqrt{0.5\lambda d}$

- Variation: proximity aligner (mask "near" substrate)

So the second approach to lithography is so-called optical lithography where you use UV light to eliminate the pattern through a mask on the photoresist. This mask is simply chrome on glass and also here you still have two main classes of lithography system. They are the so-called contact proximity aligner and projection aligner. They're shown over here so in the first one is this contact aligner where the mask is in direct contact with the photoresist. UV source generates a collimated beam and so the light is collimated in photoresist. A very simple system typically used for lab-scale systems. The resolution is determined by the wavelength and then the thickness of your photoresist and yeah, basically the distance between the mask and a photoresist. So ideally you want to keep this distance as small as possible but that has a drawback that the mask might get damaged so there is a trade-off here that should be considered. And then the projection-scale systems have projection-scale aligners. Typically you have there's a magnification involved here where the mask is actually bigger by the factor of four or five in the actual pattern that you want to write.

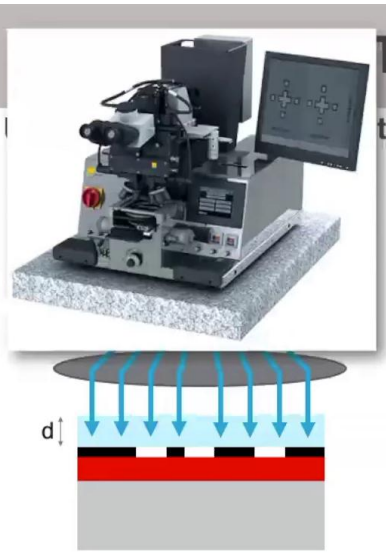
Notes

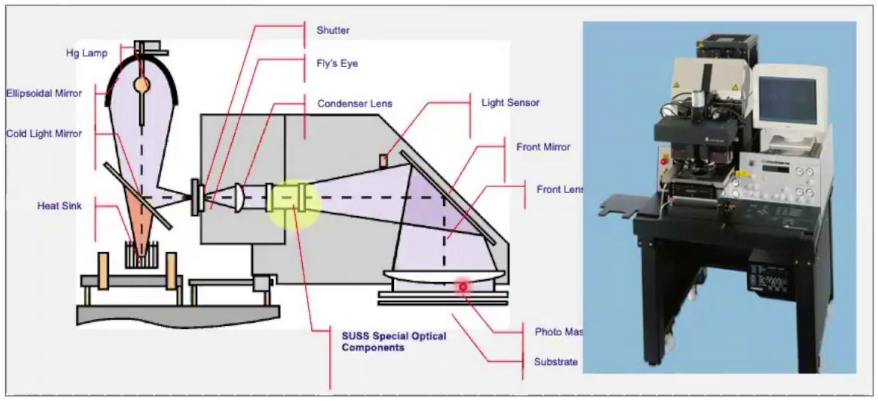
Summary

8m 56s

TICAL CONTACT LITHOGRAPHY

through suitable mask ⟹ Typically chrome on glass





- Mask in direct contact with substrate
- "Simple"
- Lab-scale systems
- Resolution: $\sim\sqrt{0.5\lambda d}$
- Alignment accuracy: optical microscope

Examples: SUSS MA6, EVG620

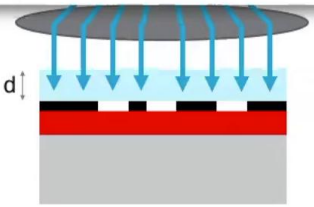
Light source:
- Hg lamp: h-line (405nm), i-line (365nm)
- XeHg lamp or excimer laser (248nm) (less common)

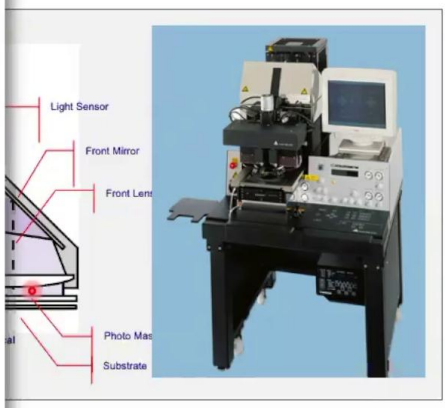
You have a projection lens over here and so the quality of that lens will determine ultimately the quality of the pattern that you want to make. The resolution is since basically the diffraction limit so it's the wavelength divided by the numerical aperture. The shorter you can make the wavelength, the higher the numerical aperture so the better the projection lens, the better the resolution. If you have a look at these optical contact mask aligners. You see an example here. A typical example from Karl Suss which allows to eliminate up to six inch wafers but also exists also systems up to eight inch. We use a mercury source to generate light at the radium of 400 nanometers maybe 365 nanometer. And that pattern is eliminated at once through a mask which has the size *[inaudible]*.

Notes

Summary

10m 13s





- Mask in direct contact with substra
- "Simple"
- Lab-scale systems
- Resolution: $\sim\sqrt{0.5\lambda d}$
- Alignment accuracy: optical microsc

620

), i-line (365nm)
ser (248nm) (less common)

You also have even smaller systems or also production-scale systems.

Notes

Summary

11m 02s

OPTICAL PROJECTION LITHOGRAPHY

Hugely complex machines, workhorse in CMOS industry

Cost: several 10MEuro

Source:

- 248nm KrF excimer laser
- 193nm ArF excimer laser
- 13.5nm Extreme UV (EUV)

$$CD \sim k\lambda / NA$$

Immersion: increases NA (and resolution)

Resolution:

- Very dependent on pattern
- Photonics: typically 180nm down to 80nm
- Overlay: few 10s of nanometer

If you want to go to really production of the CMOS industry, all systems are basically this projection type scanners. We have a very complex very expensive lens system to eliminate what happens under operation. Yeah. It's not really visible. The scale of the system is not really visible and but you have to imagine something the size of a large container. And a cost of several tens of millions that can, several tens of million euros or you can have it upgraded so if you go to the extreme UV systems. So the wavelength is very important for reaching highest resolution so the workhorse in the *[inaudible]* is now 193 nanometer resolution and more and more people also start now. Only a few companies actually start using extreme UV to have the highest resolution. You can also use so-called immersion whereby you have water between the lens and the substrate and then we're talking about immersion lithography typically in combination with 193 nanometer elimination to increase further the resolution. So resolution is very dependent on the pattern you want to write. In the CMOS industry, therefore, the order of your mask is really splitted up in in specific patterns, first one it makes all the lines and then it's all the holes.

Notes

Summary

11m 06s

OPTICAL PROJECTION LITHOGRAPHY

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Immersion: increases NA (and resolution)

Resolution:

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- Overlay: few 10s of nanometer

In photonics it is certainly not possible and that's the reason why the resolution can reach in photonics applications completely larger than the one you see for electronics application. So typically from 180 nanometers down to 80 nanometer *[inaudible]* systems. So overlay can be very crucial. We're talking about tens or even less nanometer.

Notes

Summary

12m 39s

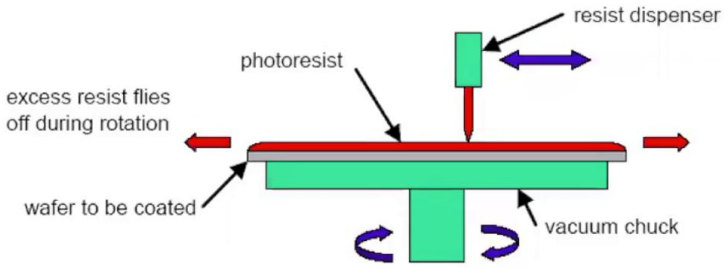
LAYER DEPOSITION: SPIN-COATING

Flexible and cost-effective method for applying resist, polymer layers …

Thickness determined by material and spin speed

Solvent in resist evaporates during spinning

Now sometimes replaced by spray coater



Next step is layer deposition. So what type of layers materials do we want to deposit? Well could be dielectrics, Silicon Oxides like Nitride, Aluminum Oxide, polymers. The semiconductors could be metals. There are many methods. We can use spin coating, chemical vapor deposition, physical deposition and also bonding and oxidation. Layer deposition through spin coating is probably the most flexible and cost-effective methods certainly for applying photoresist or polymer layers and so on. Thickness is determined by, on one hand, the material and on the other hand by spin speeds. And this material that you are gonna spin is a solvent that in a polymer layer solvent will evaporate during the spin. Basic systems can be very simple from a very cheap also a few thousand euro but you can also have very fully automated systems. Again, in CMOS industry these are the size of a full sea container.

Notes

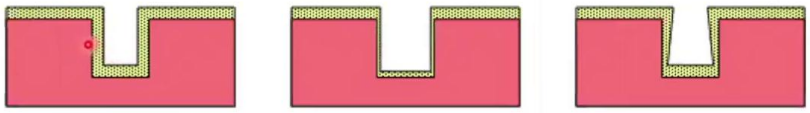
Summary

13m 02s

LAYER DEPOSITION: CHEMICAL VAPOR DEPOSITION

CVD – Chemical Vapour Deposition

- Suitable precursors are brought to substrate in gas phase and broken down
  - Using high temperature (e.g. LPCVD)(typically above 600C)
  - Using plasma processes (e.g. PECVD, ICP-CVD)(<300C, <100C)
- Important specifications:
  - Layer density, layer refractive index, layer etch resistance, thickness control, conformality
  - Amorphous or crystalline layers (epitaxial growth)



Conformal deposition K = 1 | Non ideal conformal K = 0,5 | Inhomogeneous deposition

Figure From hableiter.com

LPCVD: Low Pressure CVD – PECVD: Plasma Enhanced CVD – ICP: Inductively Coupled Plasm

Then you have chemical vapor deposition where suitable precursors are brought to the substrate in the gas phase and there they are broken down so that they can deposit on a substrate. This breaking down of the precursors can happen by using high temperature, for example, in LPCVD processes between temperatures above 600 degrees C or you can use plasma processes to bring that temperature down through Plasma-Enhanced CVD, PECVD and ICP-CVD can lower the temperature 300 degrees C *[inaudible]* You can see it still have high working hours. Important specification are the layer density, the layer refractive index, the layer etch resistance, thickness control that is possible in system conformality and so on. Just to say something about this conformality so that has to do with how uniform the position of the layer is on the top of the substrate, at the bottom of trenches and at the side of trenches. Ideally it has the same thickness everywhere but in practice, you often see that at the side of the trench or at the bottom the layer will be less thick.

Notes

Summary

14m 14s

LAYER DEPOSITION: CHEMICAL VAPOR DEPOSITION

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  - Using plasma processes (e.g. PECVD, ICP-CVD)(<300C, <100C)
- Important specifications:
  - Layer density, layer refractive index, layer etch resistance, thickness control, conformality
  - Amorphous or crystalline layers (epitaxial growth)

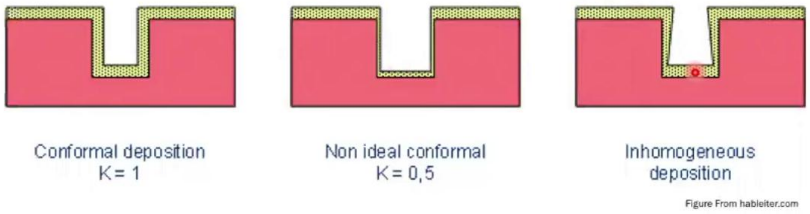


Figure From hableiter.com

LPCVD: Low Pressure CVD – PECVD: Plasma Enhanced CVD – ICP: Inductively Coupled Plasm

Very annoying situation is when you have something like this and so where you have more deposition at the corners over here because then if that layer grows thicker and thicker, it will close at the top here and the bottom will not be filled which will lead back to your holes which are often disastrous for the performance of the device.

Notes

Summary

15m 23s

LAYER DEPOSITION: CHEMICAL VAPOR DEPOSITION

CVD – Chemical Vapour Deposition

- Suitable precursors are brought to substrate in gas phase and broken down
  - Using high temperature (e.g. LPCVD)(typically above 600C)
  - Using plasma processes (e.g. PECVD, ICP-CVD)(<300C, <100C)
- Important specifications:
  - Layer density, layer refractive index, layer etch resistance, thickness control, conformality
  - Amorphous or crystalline layers (epitaxial growth)

Special case for OM: LPCVD SiN

- Si_3N_4 deposited through LPCVD method + annealing exhibits high tensile stress
- Also allows for very low waveguide loss

⟹ Great material for optomechanics !

LPCVD: Low Pressure CVD – PECVD: Plasma Enhanced CVD – ICP: Inductively Coupled Plasm

A special case for optomechanics is so-called LPCVD Silicon Nitride so if Silicon Nitride is deposited with this high temperature CVD method often followed by an annealing, that material will exhibit very low waveguide losses but also very high tensile stress. And that makes it really a great material for optomechanics and we see it in many optomechanics papers.

Notes

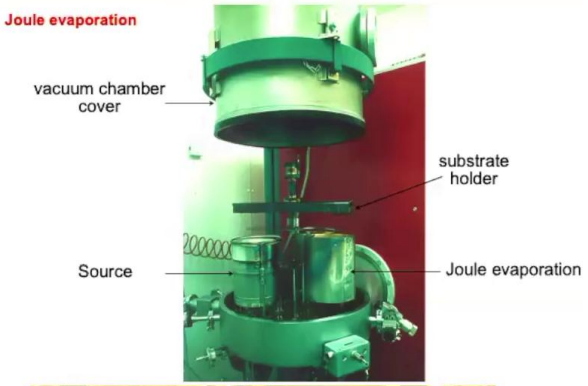
Summary

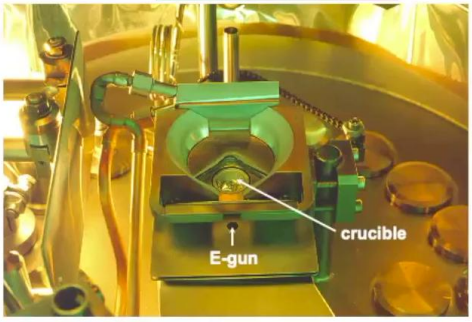
15m 41s

EVAPORATION & PHYSICAL LAYER DEPOSITION

Evaporation

- Source material is heated and evaporated towards substrate
- Joule heating or electron-beam
- Balistic process → very directional process
- Low impact





Evaporation is another and very flexible method to deposit materials and hereby the source material is heated and then evaporated towards the substrate. This heating can happen just in Joule heating by heating crucible in a resistive way or you can have in a more complex system. You can have electron-beam heating the material and locally heating it. In latter case, you need more sophisticated electronic control but it remains a very flexible process. It's a ballistic process, a very directional and it's a very low impact so you can use it also on very sensitive levels.

Notes

Summary

16m 06s

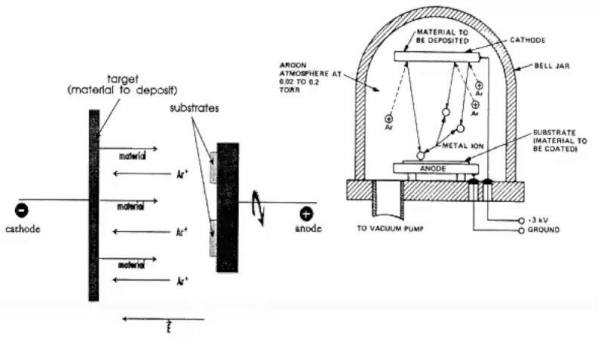
EVAPORATION & PHYSICAL LAYER DEPOSITION

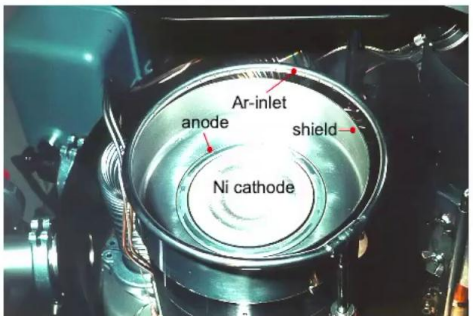
Evaporation

- Source material is heated and evaporated towards substrate
- Joule heating or electron-beam
- Very directional process, low impact

Sputtering

- Accelerated Ar-ions release material from sputter target
- Material hits device substrate
- Less directional, higher impact





An alternative is sputtering where you have accelerated argon ions, could also be other atoms, which hit your target about basically the source material, release it from the target and then until it's the device substrate. It's less directional. It has a higher impact which is sometimes a good thing, for example you want to make other impacts, it's a good thing. It can also damage more sensitive material. So it depends on what you want to do if this is a *[inaudible]*.

Notes

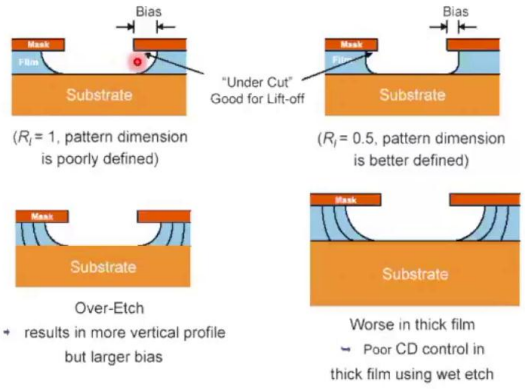
Summary

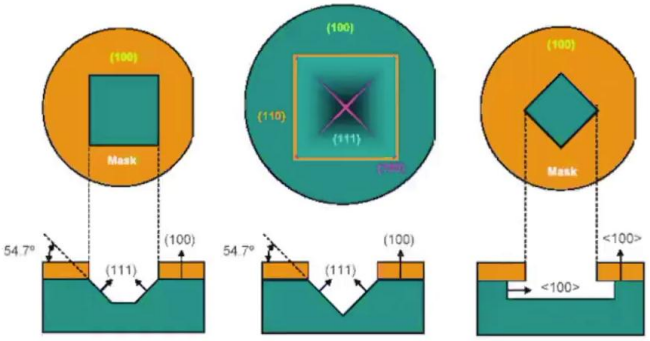
16m 44s

ETCHING

Wet-etching

- Use “wet” chemicals to etch material
- E.g. HF etches SiO_2, HCl etches InP, KOH etches Silicon, H_2SO_4:H_2O_2:H_2O etches InGaAs ...
- Important properties:
  - Selectivity
  - Isotropic vs. non-isotropic etching





Next step is etching. And again you have two main methods. The so-called wet-etching where you use wet chemicals to etch the material, for example, Hydrogen Fluoride etches Silicon Oxide, Hydrogen Chloride etches Indium Phosphide and so on. Important properties are selectivity. Is it an isotropic process or not, and so on. Here an example of the selectivity, of the selective process so here we use, for example, an etching which etches this blue layer so the bias layer with the outer edge that leaves the substrate unetched. So this is because there is a higher selectivity of the etching with respect to the substrate. Another property which is illustrated here is the difference in the etch rate between downwards and sidewards. Typically you want to you prefer a downwards etch and you want to avoid as much as possible the so-called Under Cut and to keep the highest resolution possible. However, with so-called wet chemical processes, it's often unavoidable that you have some Under Cut and that limits the ultimate resolution attainable with these processes.

Notes

Summary

17m 16s

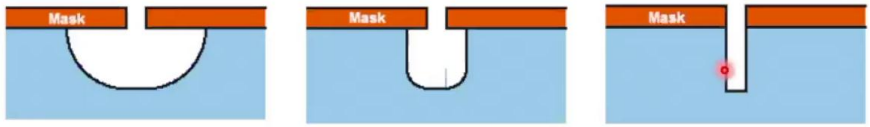
ETCHING

Wet-etching

- Use “wet” chemicals to etch material
- E.g. HF etches SiO2, HCl etches InP, KOH etches Silicon, H_2SO_4:H_2O_2:H_2O etches InGaAs ...
- Important properties:
  - Selectivity
  - Isotropic vs. non-isotropic etching

Dry etching

- Use plasma to create chemically active and high energy radicals
- Both a physical and chemical component (relative fraction can be controlled through process parameters)
- Typically higher resolution, typically more anistropic etching



R_L=1 0<R_L<1 R_L=0

That's why people started developing so-called dry etching processes where you use a plasma to create chemically active and high-energy radicals. And so in those process you have both a physical and a chemical component basically these ions are bombarding the substrate. And you can control how much physical action how much chemical action you have. And typically this will reach in a more directional etch and then the higher resolution so you can instead of having this isotropic etches where you etch the same downwards as sidewards, you can have etches where you etch only downwards and have almost no sidewards etching. So resulting in a much higher resolution. But often also sometimes in some surface damage obviously which might need to be considered.

Notes

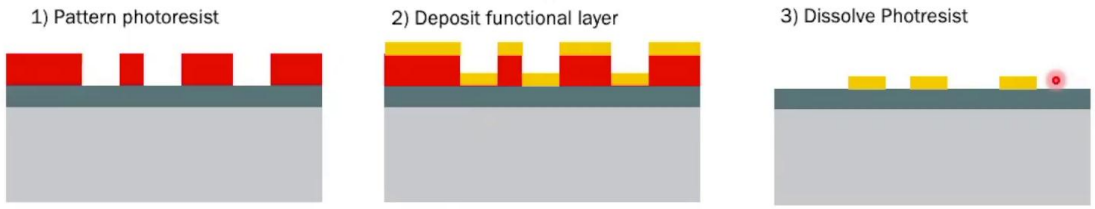
Summary

18m 33s

LIFT-OFF

Lift-off process is often used to pattern metals (Au, Ti…)

- Alternative to etching
- Some undercut in resist is advantageous



Variation, it's not really an etch process but also an important process to pattern layers is so-called lift-off process. It's often used to pattern metals actually like Gold and Titanium. So here you start again from your substrate where you pattern the photoresist and then you deposit the Gold, for example, the metal layer on top of that photoresist and if the Gold is thinner than the photoresist then the Gold on top of the photoresist and at the bottom of the trench will not be connected. So if you now put this in developer then the photoresist will dissolve and will take the Gold deposit on top of the photoresist with it and so only the Gold at the bottom of the trenches here will remain until you have a patterned layer of raw metal at the end. So this is often also a process, it's a process very often used in in metal patterning.

Notes

Summary

19m 23s

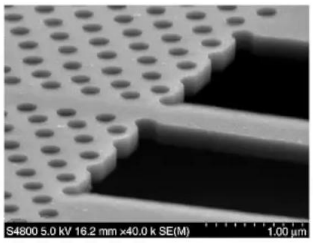
LAYER RELEASE

Layer release is essential in optomechanics !

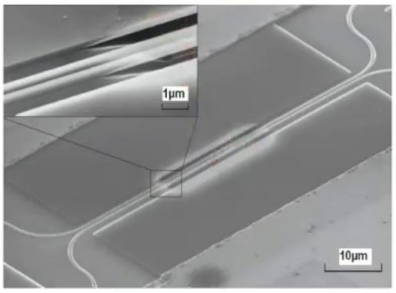
Basic approach: use wet chemical to selectively remove layer supporting functional structure

E.g. :

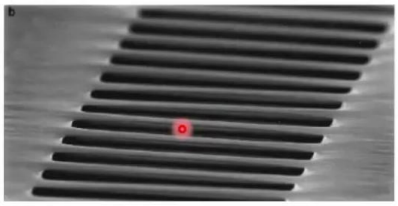
- Use HF to etch SiO_2 layer below Silicon active structure
- Use KOH to etch Silicon layer below Aluminum active structure



From physics.org



J. Roels, PhD thesis UGent, 2011



From Bo, Xiang-Zheng e.a. (2002). JAP. 91. 2910-2915. 10.1063/1.1448395.

Layer release as I mentioned it's very important in MEMS and optomechanics applications and so always you want to release your functional layer at least partly from the substrate and that here you can, it's simplest method that's used in wet chemical action to selectively remove the layer support in that functional structure. Examples you are using, for example, Hydrogen Fluoride to etch Silicon Oxide because this etch shows a very high selectivity towards Silicon which can be the substrate in the active structure or using KOH to etch Silicon below Aluminum active structures. Some examples here for number 2D photonic crystal which is free hanging and which is supported here at the sides of the structure. Here you see a support directional copper and two Silicon beams which are locally under edge so here the oxide support has been removed. This is another example here of beams. Actually a more of silicon *[inaudible]*. You see these pictures and if you make PowerPoint drawings, this all looks very easy.

Notes

Summary

20m 22s

LAYER RELEASE

Layer release is essential in optomechanics !

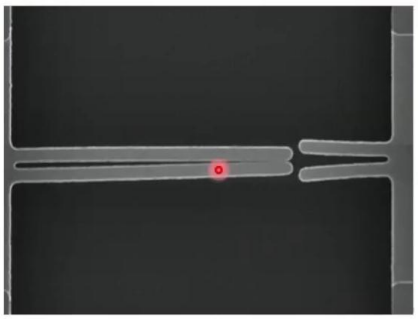
Basic approach: use wet chemical to selectively remove layer

E.g. :

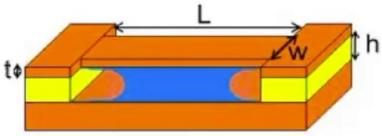
- Use HF to etch SiO_2 layer below Silicon active structure
- Use KOH to etch Silicon layer below Aluminum active structure

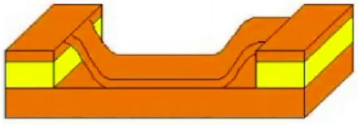
Problem !! Collapse and stiction

- When drying liquid etchant, surface tension results in downwards force pulling structure towards substrate

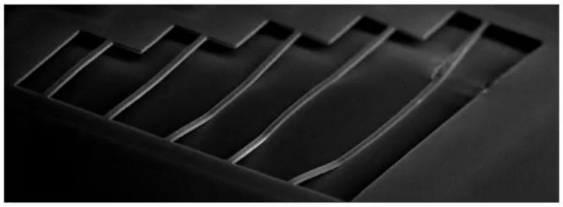


J. Hakansson, PhD thesis UGent, 2019





J. Roels, PhD thesis UGent, 2011



J. Roels, PhD thesis UGent, 2011

In practice, however, it's far from being that easy. Many cases you will suffer from so-called collapse and stiction. It is related to the fact that when you dry the liquid etchant, surface tension might cool down and the beam here towards the substrate and result in stiction of that beam towards the substrate so you can see that very very well here. With the shorter beams which are stiffer basically are free hanging but then the longer beams they are all touching the substrate and you are stuck there and basically these structures are like this. Your structures can be stuck to the substrate but they can also be stuck to each other as you see here in this example where two beams are touching each other *[inaudible]* You can solve that by using stiffer structures, for example, this highly strained Silicon Nitride or smaller structures.

Notes

Summary

21m 34s

LAYER RELEASE

Layer release is essential in optomechanics !

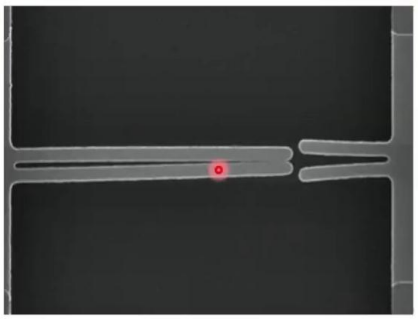
Basic approach: use wet chemical to selectively remove layer

E.g. :

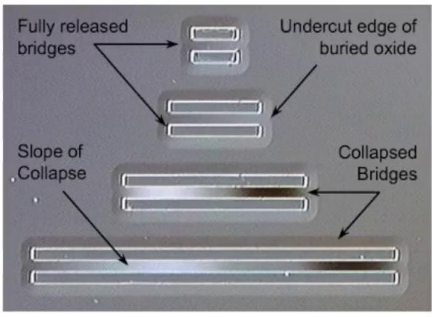
- Use HF to etch SiO_2 layer below Silicon active structure
- Use KOH to etch Silicon layer below Aluminum active structure

Problem !! Collapse and stiction

- When drying liquid etchant, surface tension results in downwards force pulling structure towards substrate
- Solution:
  - Use stiffer structures (highly tensile strained SiN, smaller structures ...)
  - Use critical point drying (CPD)
  - Use dry etching methods (Vapor HF for SiO_2, XeF_2 etching for Si ...)



J. Hakansson, PhD thesis UGent, 2019



JVSTB **28**, 1195 (2010)
https://doi.org/10.1116/1.3503612

You can use a technique called Critical Point Drying or you can use dry etching methods like Vapor HF for Silicon Oxide and Xenon Difluoride for etching Silicon. We avoid this liquid phase altogether.

Notes

Summary

22m 28s

BONDING

Bonding allows to combine high-quality materials that cannot be deposited otherwise

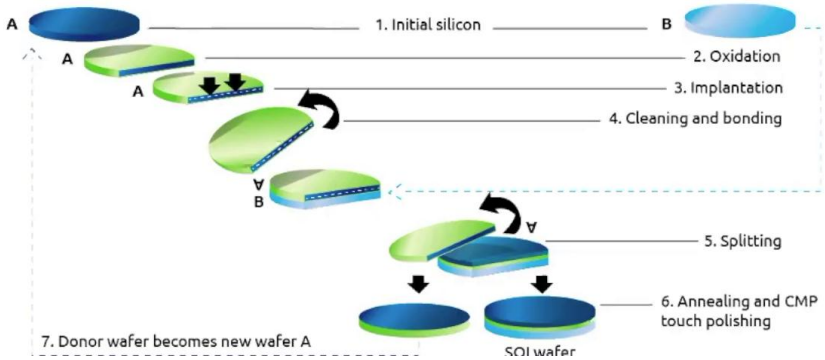
- E.g. crystalline materials with different lattice constant, partially processed layers ...

Many variations

- Direct bonding, molecular bonding, adhesive bonding
- Wafer to wafer, die-to-wafer, transfer-printing...

Examples:

- SOI, III-V on silicon, Lithium-niobate thin film ...



Finally, bonding and planarization. Bonding is a process that has in the last decade become more and more important, in general, in micro and nanofabrication techniques in many domains but in particular, also in optomechanics and *[inaudible]*. It allows us to combine materials that cannot be deposited from each other otherwise. For example, crystalline materials with a very different lattice constant or partial processing. There's many variations. You can have direct bonding, molecular bonding, adhesive bonding. You can have wafer to wafer bonding where one can see fluid waves that can also bond small dies to free layers so you can have process called transfer-printing where you can print many small dies simultaneously. The most well-known example is a wire or Silicon-on-insulator which is actually fabricated by bonding two silicon wafers together and then release the substrate for *[inaudible]* using the so-called Smart Cut method. It's also used within the open photonics for integrating three-five so direct band gap same connection in Silicon photonics waveguides.

Notes

Summary

22m 42s

BONDING

Bonding allows to combine high-quality materials that cannot be deposited otherwise

- E.g. crystalline materials with different lattice constant, partially processed layers …

Many variations

- Direct bonding, molecular bonding, adhesive bonding
- Wafer to wafer, die-to-wafer, transfer-printing…

Examples:

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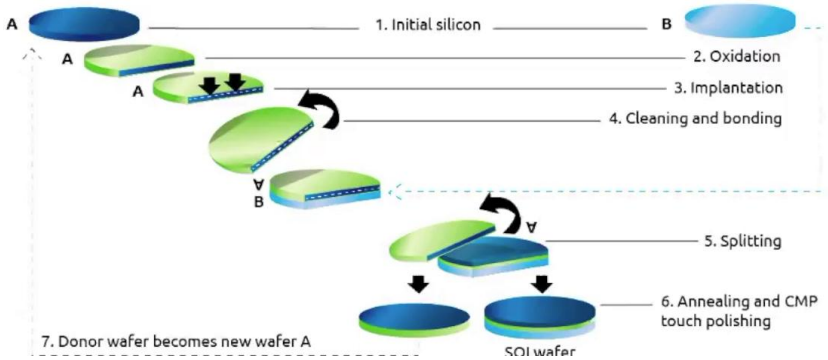
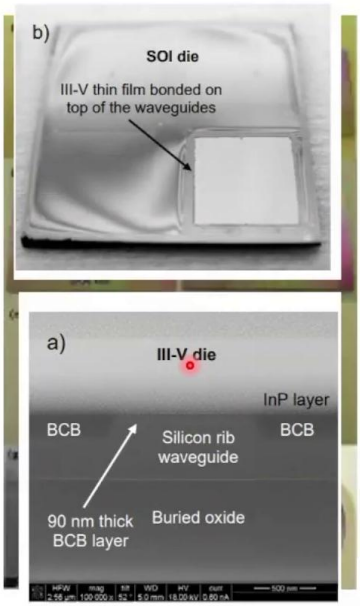




Some examples here that you see, for example, a three-five film bonded on top of Silicon waveguide and here you see a cross-section of *[inaudible]* so we have a three-five here made of Silicon and a thin layer of polymer in between which is actually the blue color. So then, of course, you can make the laser in three-five die and *[inaudible]* the light through the Silicon. You could say that why don't we directly deposit the three-five from the Silicon but obviously most three-five materials have four to eight percent lattice mismatch with Silicon so direct growth of three-five into the Silicon, it's very challenging. And so these bonding methods are *[inaudible]*.

Notes

Summary

23m 49s

PLANARISATION

Device processing results in un-even surface

Planarisation in many cases essential

- Maintaining resolution in next process steps
- Bonding
- Deposition of thin layers, e.g. through spin coating

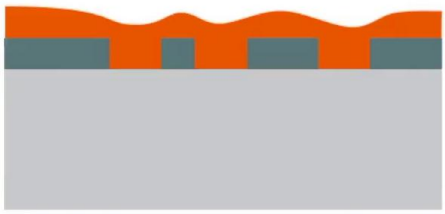
Poor man's approach:

- Spin coating thick layer & etch back (BCB, spin-on-glass…)

Better approach:

- CMP – Chemical Mechanical Polishing
  - Thick oxide deposition
  - Mechanical polish down (with some wet chemical support)
- Difficult on samples, pattern dependent,..
- Key in industry, challenging in lab environment

Spincoated layer to partially planarize substrate



Substrate planarized with CMP

Before bonding you often need to planarize your substrate. So planarization is also becoming more and more important. Also for other reasons planarization is also important if you want in the overall resolution under processing or if you want to deposit thin layers through spin coating. The Poor man's approach to planarization is same as the approach you used in lab-based processing. It's often spin coating a thick layer and then etch it back *[inaudible]* if you start with the pattern device layer and then you spin coat a polymer on top of it. Some of the some of the topography will be washed out by spin coating this layer and then actually you can repeat this several times till you have something which is more of a skin. And then if the layer becomes too thick you can etch it back to have something which is planarized close to the original substrate. This works but it has limited control. A better approach is so-called CMP or Chemical Mechanical Polishing but again you deposit a thick oxide in most cases and then you mechanically polish it down often with the help of some wet chemical. That wet chemical can be as simple as just using water.

Notes

Summary

24m 34s

PLANARISATION

Device processing results in un-even surface

Planarisation in many cases essential

- Maintaining resolution in next process steps
- Bonding
- Deposition of thin layers, e.g. through spin coating

Poor man's approach:

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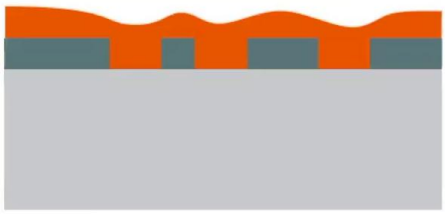


Substrate planarized with CMP

[inaudible] Unfortunately, well the good thing is that, that leads to much better planarization much higher quality and it's really a key process that we see more limits. Unfortunately, challenging in a lab environment, it's difficult on small samples, it's very pattern dependent, it's often avoided in the lab.

Notes

Summary

25m 54s

A NOTE ON "CMOS COMPATIBILITY"

The term "CMOS compatible" is (mis)used in a lot of papers as a motivation

It can mean anything, depending on who you talk to:

- Fabricated in a clean room...
- Processed using planar fabrication technologies
- Processed at temperatures compatible with CMOS-electronics (<400-550C)
- Using only Silicon/SiO_2
- ...
- ...
- Processed in a CMOS-pilot line (imec, CEA-LETI)
- Processed in a CMOS-fab (ST, TSMC, INTEL...)
- Zero-change CMOS (e.g. MIT @ Global Foundries)

Most important: it can be processed on a silicon substrate

Okay, this brings me to the end. Just some concluding remarks. If you, first a note on so-called CMOS compatible. So if you start reading many papers nowadays, it will start with saying, ah, my processing is CMOS compatible so it is important. My opinion this is misused in a lot of cases and can basically mean anything so in some cases it just means it's fabricated in clean room. In other cases, it's very slipped and means that it's really fabricated in a CMOS-fab without the people doing the the fabrication more it is about optomechanics or optics. So it can be anything in between there so actually the actual meaning is just disappeared. For me what is important is probably mostly that it can be processed on a Silicon substrate and that's the reason for that is that these substrates are very important for the machines which are handling which are used to support your functional layers and so all these machines are relying on the substrate that they're handling. This is very stiff for certain dimensions. The Silicon substrates are the most important but otherwise almost anything if it gets important enough it will be made CMOS compatible.

Notes

Summary

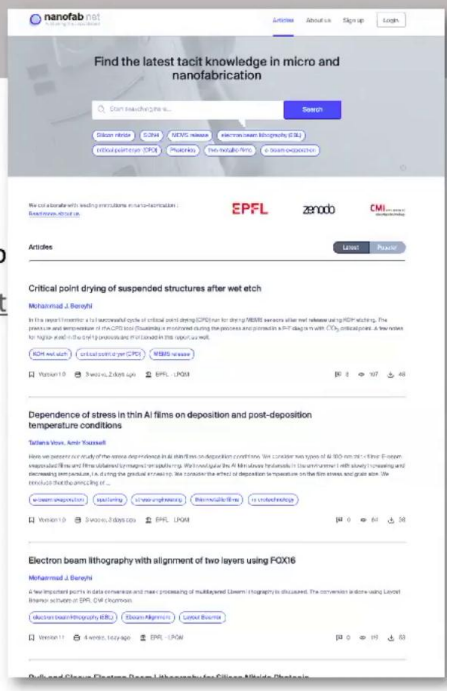
26m 18s

ACCESS

How do you get access to all these technologies ?

Option 1: you have your own cleanroom

- Great !
- But process development is very time consuming. A lot of time might get lo
- A lot of “hidden” know-how. Share your experience on https://nanofab-net



The other final note I want to discuss here is access. How do you get access to all these technologies? Well, the ideal case the first option is you have your own clean room or at least your university has its own clean room. Well, that's great. The challenge and what you have to take into mind is that process development can be very time consuming. A lot of time might get lost in the basics. For example, you might lose a lot of time in just developing a good waveguide before you can do any real science. Also there is a lot of hidden know-how and so the papers never say everything and might cost you a lot of time to discover that hidden know-how. To resolve that actually some people at from OMT and all projects at the EPFL started to sharing their experience here on this website. I’ll show the screenshot over here where they really have the intention to share this hidden knowledge and also invite other people to support to submit specific cases of specific processes with all parameters and not just selected parameters. So I encourage you if you have these kind of processes developed also to share them.

Notes

Summary

27m 43s

ACCESS

How do you get access to all these technologies ?

Option 1: you have your own cleanroom

- Great !
- But process development is very time consuming. A lot of time might get lost in “basics”...
- A lot of “hidden” know-how. Share your experience on https://nanofab-net.org

Option 2: you do not have your own cleanroom

- Use MPW-services (Multi-Project Wafer)
- Available for Silicon Photonics (imec, Leti, Southampton...), Silicon Nitride (Lionix, imec, Ligentec...) and III-V (TU/e, HHI...)
- https://europractice-ic.com, https://mycmp.fr, https://www.jeppix.eu, https://www.cornerstone.sotonfab.co.uk

Option 3: Combine MPW-services with your own processing !

Second option is so-called use of multi-project wafer services MPW services. These are now available, for example, for Silicon Photonics, for Silicon Nitride and of course, also for electronics, in general. You can access them from many websites. Very widely valued price points also you can obtain them. The third option and maybe the best one or the most advantageous one in my opinion is actually combining these two with starting with a chip you get from an MPW service where you get the basics done and then you do your own processing your own science and automations. But that just might be. Okay. Let's conclude this session.

Notes

Summary

29m 07s