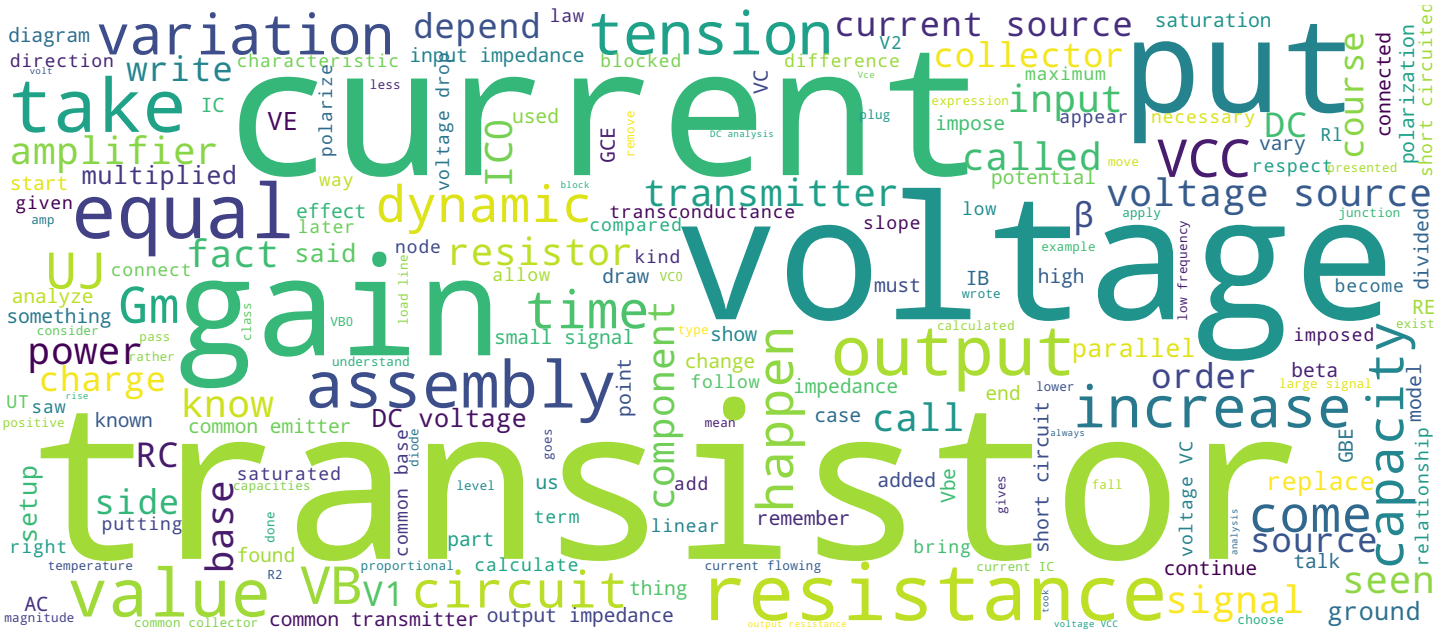
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

5.2-Amplificateurs élémentaires à transistors

Amplificateurs de tension

Prof. Maher Kayal

Electronics Laboratory-ELAB



Video

EPFL

Introduction

- Schéma petits signaux de principe
- Schéma grands signaux
- Schéma complet avec l'ensemble des composants
- Critères de dimensionnement.

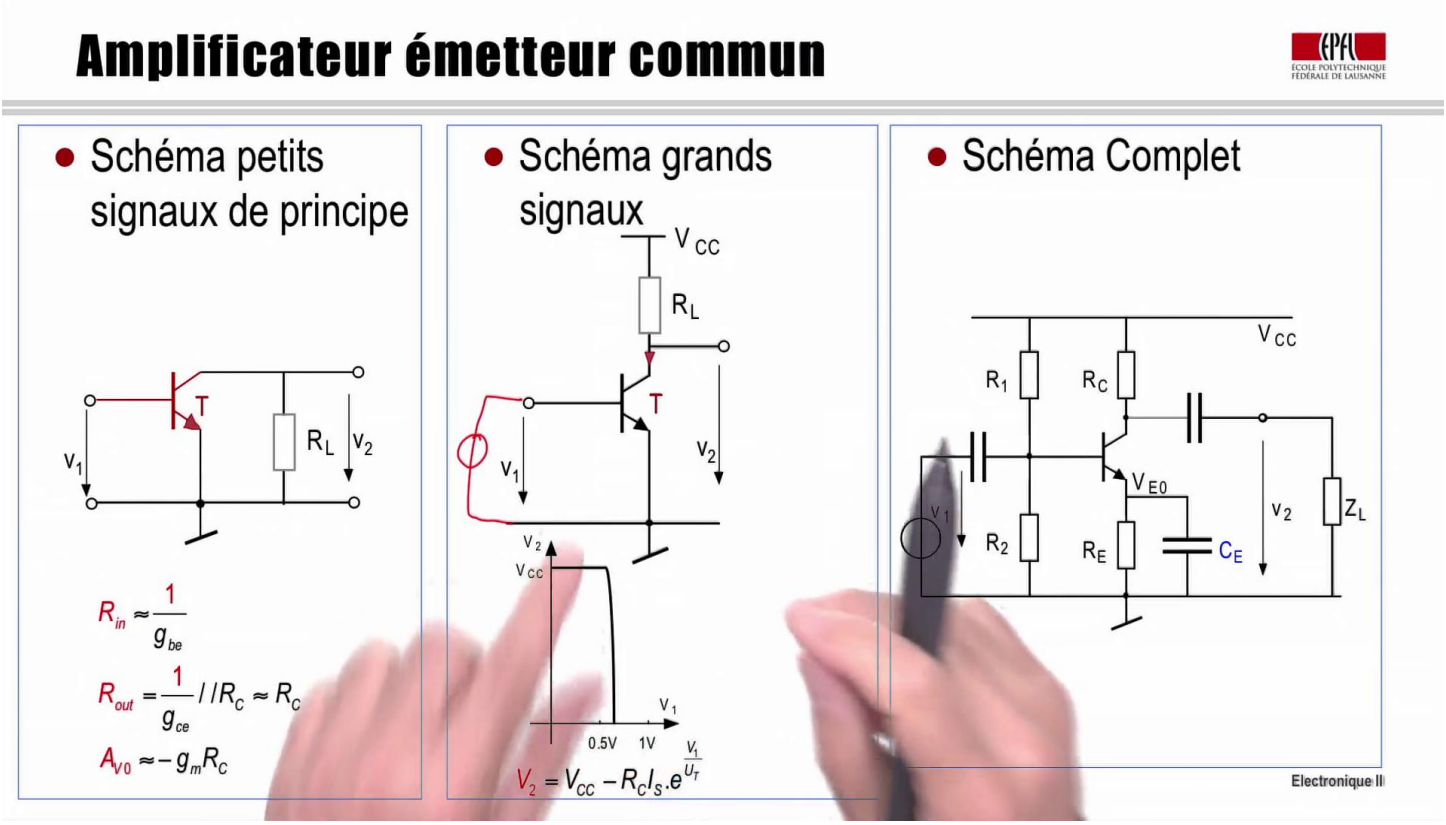
Electronique II

So in the continuation of what we have just seen, we will now analyze a real implementation and analysis of this emitter-common mounting with the components we have just seen which are essential for the use of this amplifier when it is realized as an AC amplifier. So let's look at how do we analyze an assembly with 3 resistors and 3 capacities we would have added for the coupling and decoupling and the polarization that will be the subject of this part and then we continue with the analysis of what is called he elbow break mounting which is an improvement of this assembly voltage amplifier realized using a common emitter.

Notes

Summary

0m 05s



So as presented that it always revolves around the common emitter also presented as it will turn around this polarization there, here to the right, you have the famous full scheme which was presented just before and we saw the 3 capacities which had to be added and we had seen that the difference between this assembly and its small signals scheme and the fact that this capacity allows to connect the transmitter to ground and that this capacity, it brings us back to what we had already studied before and the input impedance and the output impedance, the gain this is what is now known by any student who had taken the course from the beginning. In the center, I present what I call the great scheme signals. The major pattern signals is that you take the common emitter and connect between the base and ground a source of DC voltage, so I insisted on the fact that this is a DC source. And I vary the DC voltage from 0, therefore the voltage V1 I vary from 0 to VCC and you will see that your transistor count voltage V1 equal to 0, so this is short-circuited here the transistor is blocked. And when a transistor is blocked, no current flows therefore this tension equals to this one.

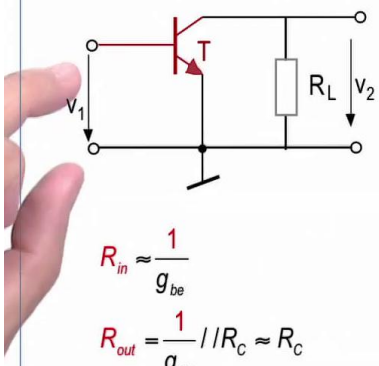
Notes

Summary

0m 50s

Amplificateur émetteur commun

- Schéma petits signaux de principe

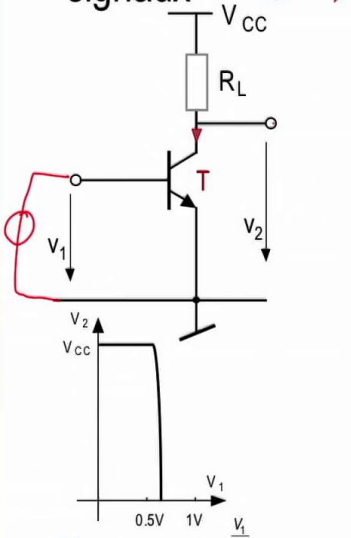


$$R_{in} \approx \frac{1}{g_{be}}$$

$$R_{out} = \frac{1}{g_{ce}} // R_C \approx R_C$$

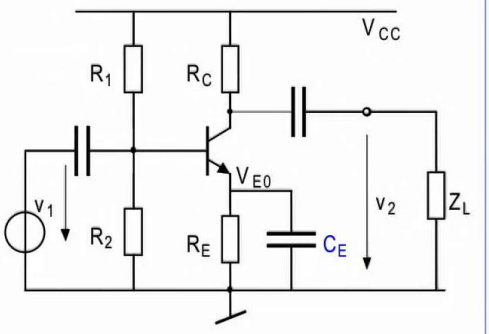
$$A_{V0} \approx -g_m R_C$$

- Schéma grands signaux (DC)



$$V_2 = V_{CC} - R_C I_S . e^{\frac{V_1}{U_T}}$$

- Schéma Complet



Electronique II

When there is no current which passes through this resistance there is no voltage drop at the edge of this resistance, this node will copy the voltage VCC. And if you start to increase the DC voltage here you will see that the transistor comes out of the blocking around the junction voltage and after you are going to have the exponential transistor law precisely because we plugged in the transmitter to ground. We call this type of representation large signals pattern or it is called DC analysis when you make a "spice" simulation to see the same thing you must go to see a DC analysis by putting a source of DC voltage at the input. If we rather want to look at this, it will be necessary to put an AC source and if you take the complete pattern and you take away the capacities, the DC analysis is by plugging a DC voltage source here instead of those 2 resistances and the AC analysis is by putting an AC source here and looking at the change in this node which corresponds to an AC node, but the pattern small signals of C2 if the decoupling capacity CE is well calculated, it would amount to the same assembly therefore that gain one.

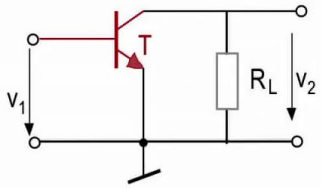
Notes

Summary

2m 23s

Amplificateur émetteur commun

- Schéma petits signaux de principe



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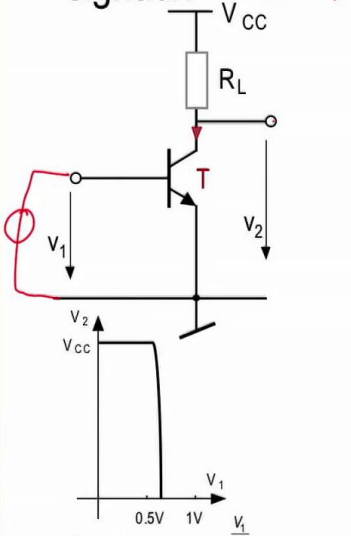
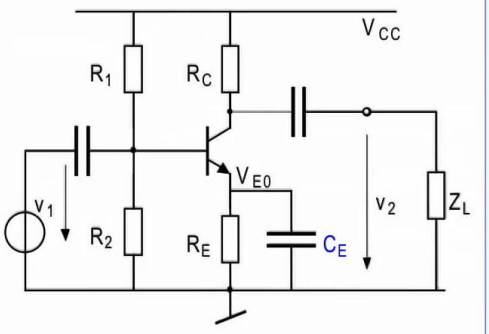
- Schéma grands signaux (DC)



$$V_2 = V_{CC} - R_C I_S . e^{\frac{V_1}{U_T}}$$

- Schéma Complet



Electronique II

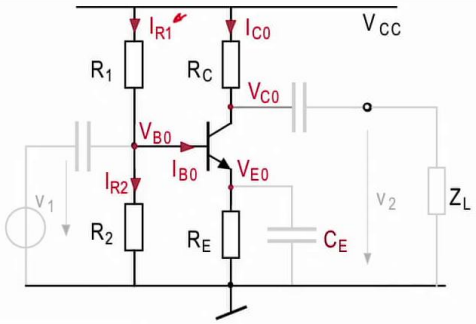
So in this chapter I will go through the analysis in detail of this assembly and go step by step to understand all the laws that allow us to dimension it in any case analyze it through the 3 modes of DC analysis point of operation followed by large signals analysis therefore DC and terminated by the small signals scheme.

Notes

Summary

3m 41s

Point de fonctionnement



$$I_{R1} \approx I_{R2} = \frac{V_{CC}}{R_1 + R_2} > 10 I_{B0}$$

$$V_{B0} \approx V_{CC} \frac{R_2}{R_1 + R_2}$$

$$V_{E0} = V_{B0} - U_j$$

$$I_{C0} \approx I_{E0} = \frac{V_{E0}}{R_E}, I_{B0} = \frac{I_{C0}}{\beta}$$

$$V_{C0} \approx V_{CC} - I_{C0} R_C$$

$$g_m \approx \frac{I_{C0}}{U_T}$$

$$g_{be} \approx \frac{I_{C0}}{\beta U_T}$$

$$g_{ce} \approx \frac{I_{C0}}{V_A}$$

Electronique II

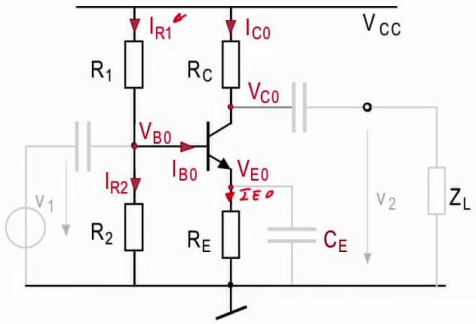
Here it is ! The first thing, that anyone who sees a pattern of that style having known values R1, R2, RE, RC, everything is given, you can immediately calculate all the parameters needed to analyze this scheme. The potential VB0, as analyzed before, we hide the assembly and we consider IB0 almost negligible therefore it is neglected, we can neglect it provided that we imposed a current IR1 significantly higher than IB0, it has already been explained. So if you take IR1 of the order of ten times IB0, you can safely consider that this is anything other than a conventional resistive divider. Hold you take the voltage VCC, you lower it to VB0 by putting two resistors R1, R2 of your choice and these two resistors must obey the fact that the currents passing through them, it is still 10 times higher than the current that your assembly will take. And it allows you to write after this VBO law and you put the... so you choose your VB0 and you write the relationship of a resistive divider. Now the VE0 voltage, it's the same thing that VB0 dropped of UJ which appears between base and emitter of this transistor. That's it !

Notes

Summary

4m 08s

Point de fonctionnement



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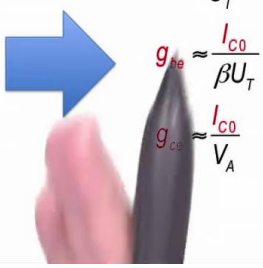


Electronique II

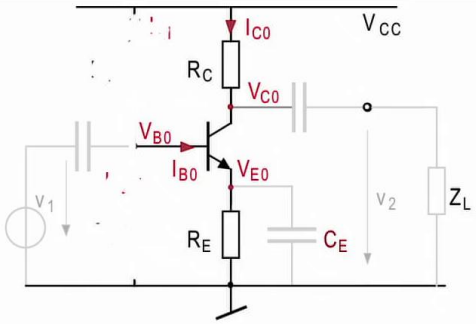
This transistor contains everything needed to obtain a current IE0, this current IE0 which is the same as IC0, we get it through this resistance. So VB0 minus UJ divided by RE gives us the IC0 current, and there we can deduce what is the current IB0 and it would give us this relationship. Of course one must know the beta of the transistor. And that's it, we have the value of VC0 because IC0 is given. We have the value of the load resistance, it gives us directly what the potential VC0 is. Someone who has done this systematic approach knows, there is nothing to do, it's called the operating point or the resting point of this assembly and by analyzing it if we have the values, it is traversed in this way. If we do not have those values, we have to go in that direction. It is necessary to impose IC0, know the current that will be used to polarize and make the steps in this direction. That is what will give us what is the tension that we need to impose and in this case calculate R1 and R2 values such that their sum allows a current which traverses them IR1 to be higher to 10 times IB0. But once we did that, we can pass on AC analysis.

Notes

Summary

5m 36s

Caractéristique Grands signaux (DC)



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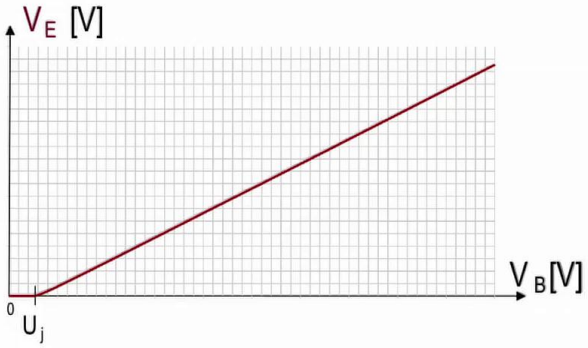
$$g_{be} \approx \frac{I_{C0}}{V_A}$$



Electronique II

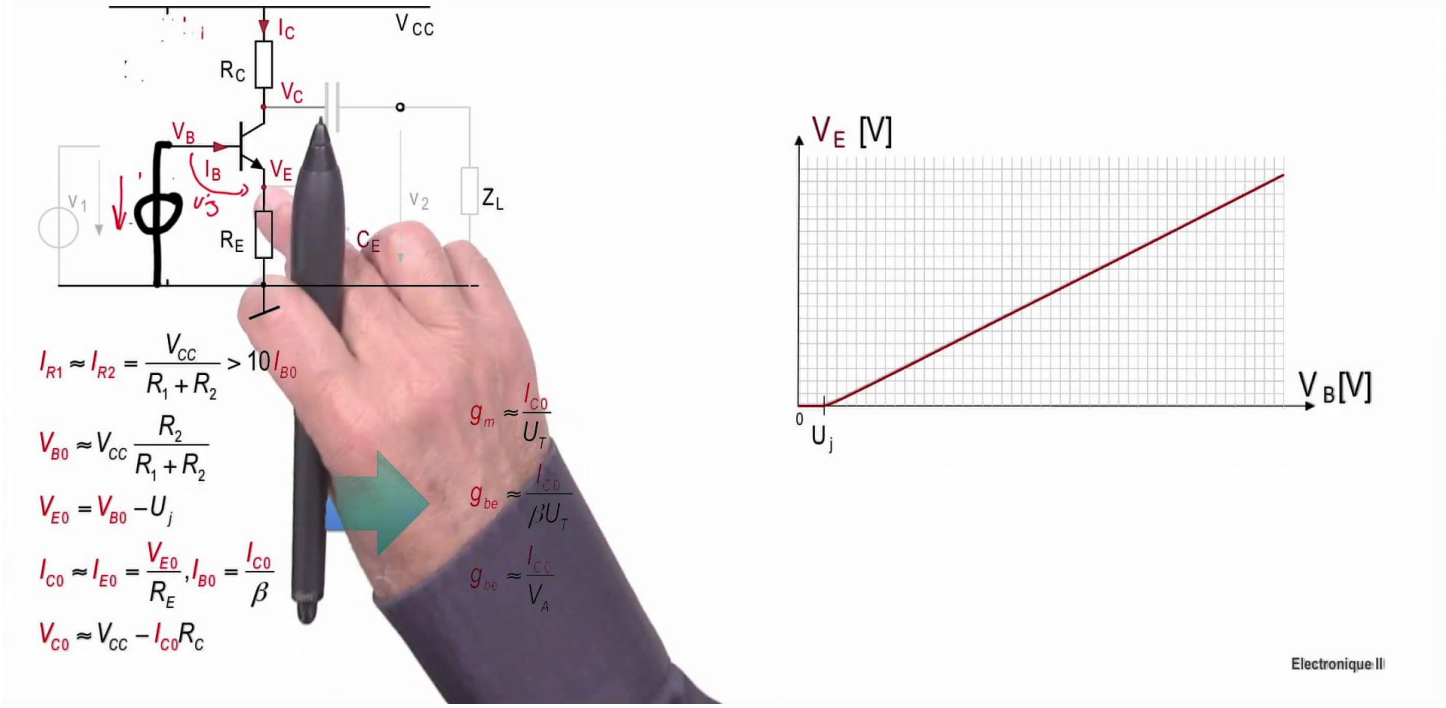
The AC analysis means you need to know everything that concerns your transistor when you take it off and you put in place a small signals diagram we will see just now, it is the GM, the GBE and the GCE which depend on this IC0 we just imposed and analyzed by this scheme otherwise UT is known 26 millivolt, beta of the transistor is known, VA is the Early voltage, Therefore the GM, GBE, GCE arise from the fact that IC0 is imposed. We will analyze the characteristics and large signal of such an assembly. So I repeat here you have the point of operation, here you have the AC settings of your transistor and we will look to what is happening with this montage if there has not been this resistance which is there, so I'll erase the resistance that is here. This resistance which is here we will delete it and same for the resistance of the top, it does not exist and we will replace them, this resistive divider by a real... by a real assembly with a voltage source that will connect here. So I'm going to draw a voltage source but I'm going to eliminate these capabilities because they are useless and we will look at what will happen with all that variation of potential content of this transistor when a DC type voltage source is connected there, so I plug here a DC voltage source and this DC voltage source I call it VB because it is directly connected to the base of this transistor.

Notes

Summary

7m 08s

Caractéristique Grands signaux (DC)



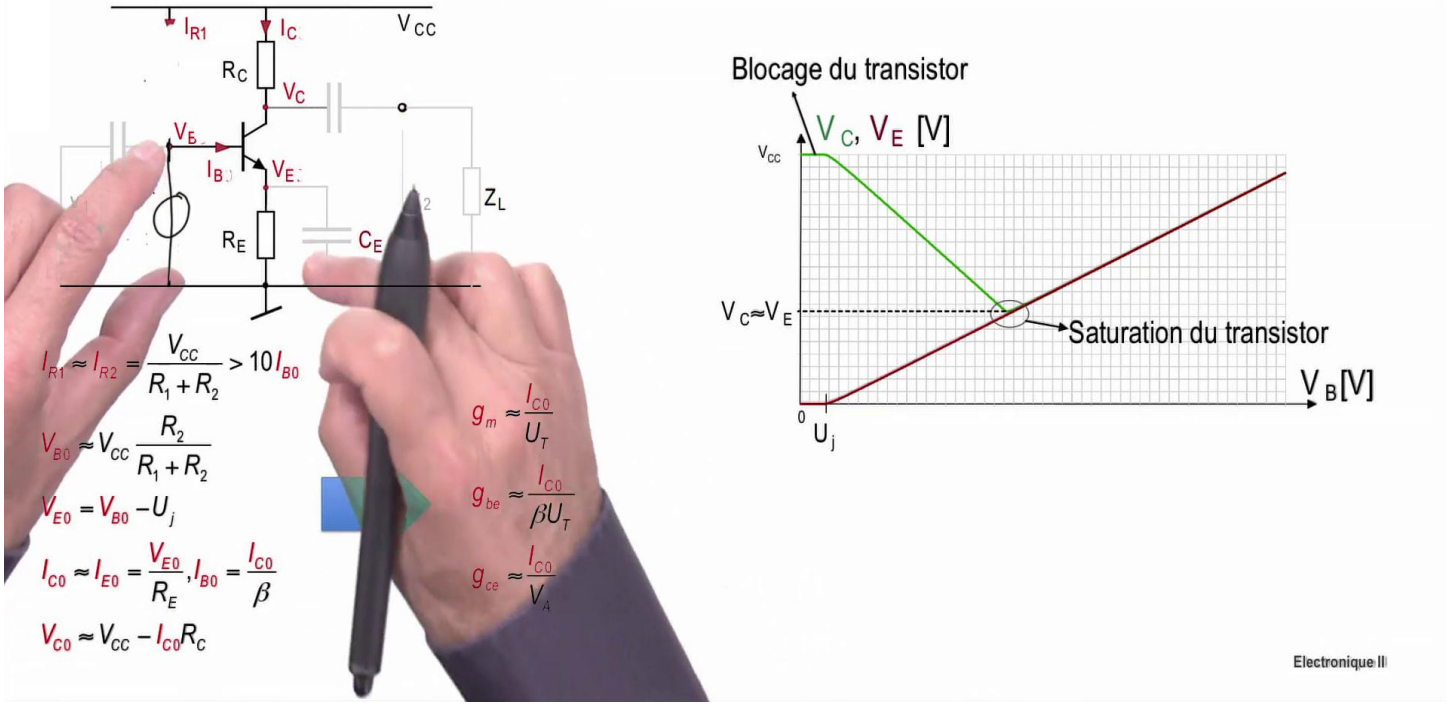
And I will vary the voltage source from 0 to VCC and observe what will happen with VE, VC in VB we known that is the source itself and that, it allows us to see the large signals, the characteristics large signal or in other words, the test analysis of such a assembly. Of course the capabilities, they can remain or be eliminated it doesn't change anything. Because these capacities face to face a test variation does not intervene at all on what we will see on that node then that node or that. We come to the assembly as seen with an input VB, an output VE, these 2 tensions follow on another. Everything you put on the VB, it copied them on the VE with a voltage drop is equal to UJ So you have a voltage drop here: of the UJ and this voltage of variation account, come up or down that it absolutely follows is what we see here. It is necessary that the transistor must be greater than VB UJ so that the transistor comes out of blocking, so there my transistor is off, here my transistor is off and then after VE will absolutely follow the variation of VB. So this is a right that has a slope of 45 ° because VB and VE are... we also call a follower transmitter because the transmitter follows the variation of what they put him as voltage based.

Notes

Summary

9m 05s

Caractéristique Grands signaux (DC)



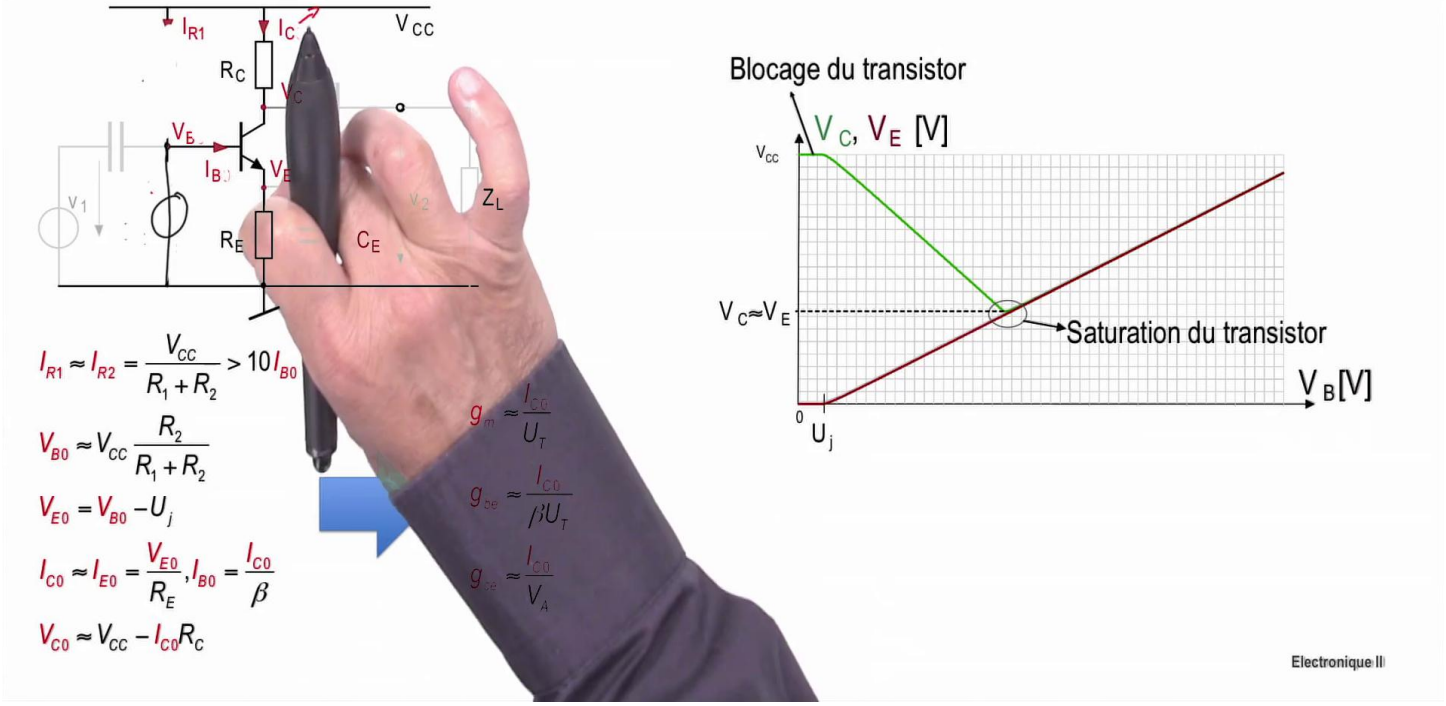
We'll now pass to observe what will happen with VC. I repeat the same pattern, and I look at the potential VC. We saw VE and we want to see what happens with VC. How it behaves this transistor? So you remember that I already erased my resistance, my resistance no longer exist, these resistors there are erased, I remake on this new slide not to disturb you, I delete it, there is no such resistance and then I replace by a voltage source VB. And I quickly added my voltage source here which is VB and I'll observe what will happen to the output to know on VC because the output is considered VC, I go out on the collector. I go out on the collector, I see here a slope which corresponds to the following: when you have a VB voltage here that starts from 0, VE will follow her, I increase the VB voltage I will have the transistor which comes out of the blockage So VE copy VB, we see him increase at the same time he will be a current IC which will start in the transistor and the more I increases the voltage VB, I'm increase VE so I'm trying to increase IC with, why? Because it's VB minus UJ divided by RE it gives IE and this IE is exactly IC so I have a voltage which rises at the same time, this current then increases at the same time.

Notes

Summary

10m 36s

Caractéristique Grands signaux (DC)



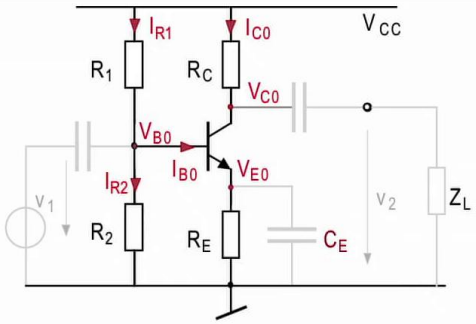
So this current here, it is currently increasing at the same time. Look, when you increase the IC current what's happening with this tension beside RC? so the voltage VC decreases with, more IC increases, the VC voltage approaches the ground. So if you measure the voltage VC with respect to ground this is usually done, we put a voltmeter with a tip here and observed VC and we will see that VC is diminishing. so we will see that most VB increases, IC increases, VC decreases, which is why we have the minus sign in a transistor when looking at his gain, we say that VC is in the opposite sense that VB, there is a delay of 180 ° when is about a sinusoidal voltage. And look what is happening there. I see VC coming down that goes down and it goes down until when? You see VE increases, VE is going up and VC is going down and there we have a transistor between the two, a transistor when VC equals to VE, it saturates. And in reality, in practice, it saturates before VC equals 0, but there VC will go down, VE is going up and it will reach the saturation of this transistor and when a transistor saturates the linear region using your amp does not exist.

Notes

Summary

12m 26s

Point de fonctionnement/repos et Grands signaux



$$I_{R1} \approx I_{R2} = \frac{V_{CC}}{R_1 + R_2} > 10 I_{B0}$$

$$V_{B0} \approx V_{CC} \frac{R_2}{R_1 + R_2}$$

$$V_{E0} = V_{B0} - U_j$$

$$I_{C0} \approx I_{E0} = \frac{V_{E0}}{R_E}, I_{B0} = \frac{I_{C0}}{\beta}$$

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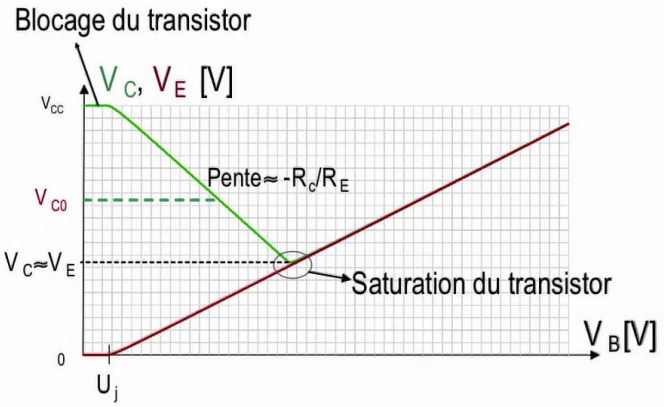


Electronique II

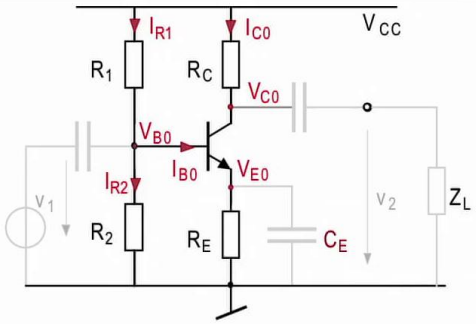
There, any variation in VB versus VC, apart from the fact that it is a negative sign, we just explain and well we see that there is a linearity well this linearity is a gain with a negative sign that has some value. But as soon as the transistor saturates, this tension becomes like a circuit there, short circuit, it is short-circuited here, so he has no more this effect. We'll see VB and VE which continue to follow, but your transistor will see RC and RE at the exit that affect and you have an IC current here which will be dominated by the current flowing through the base. So this current, it can not more grow, he continues on his way, it adds to IB the current so IE is not equal to IC on the contrary because it is more IB which will increase the current RE in resistance rather than IC. But what I would say, the transistor go from a blocked situation and it will reach the situation where the transistor is saturated. And right now, I would put everything flat and look at what happened with my assembly the layout editing here showed me all that will happen with my transistor conducts and impose DC voltages, there is no variation, I am not at all interested with an AC signal.

Notes

Summary

13m 49s

Point de fonctionnement/repos et Grands signaux



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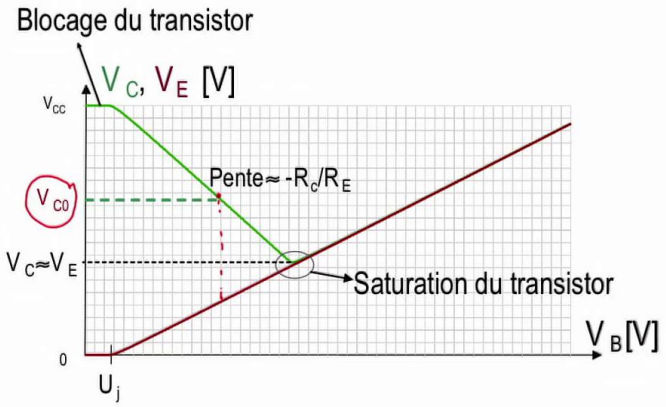


Electronique II

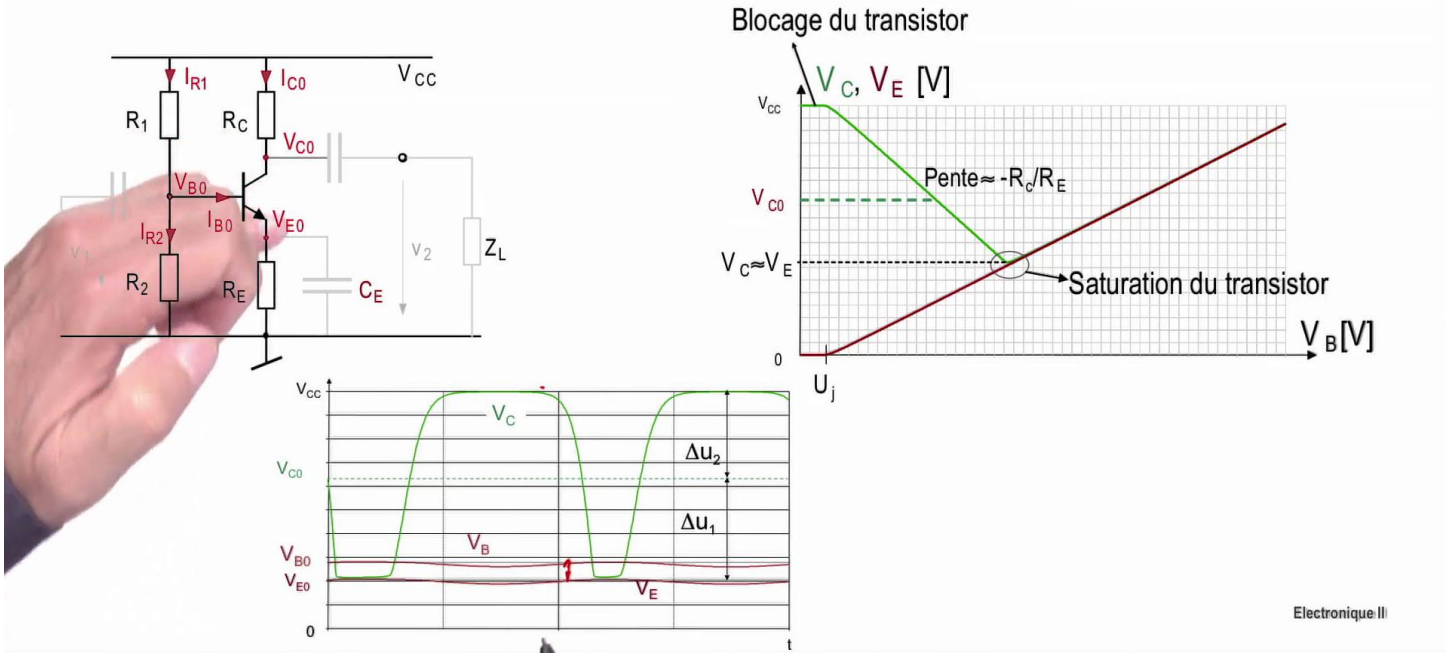
I am especially interested at a DC behavior of this transistor and in this case, there is a particular point, that is this transistor then when I realized I put a resistor R1 and R2 to polarize and I found the VC0 tension there, that's the VC0 voltage, for voltage VC0 of course I have a voltage VE0 on this curve there which corresponds to a current flowing through my transistor. And there is a variation in VC compared to VB which is a straight, what is the slope of this line? This is - RC / RE so the exercise we treated outside this video on RE on RC which demonstrating that the gain is equal to RC / RE seen here. I, I've mentioned before to say the gain equal to - RC / RE. Well this is a gain fairly linear because It is a ratio of 2 resistances, if you put RC larger than RE, it is a gain as seen here with a negative sign because there is the fact that VC decreases as VE increases, Sorry, forgiveness that VB increases.

Notes

Summary

15m 14s

Point de fonctionnement/repos et Grands signaux



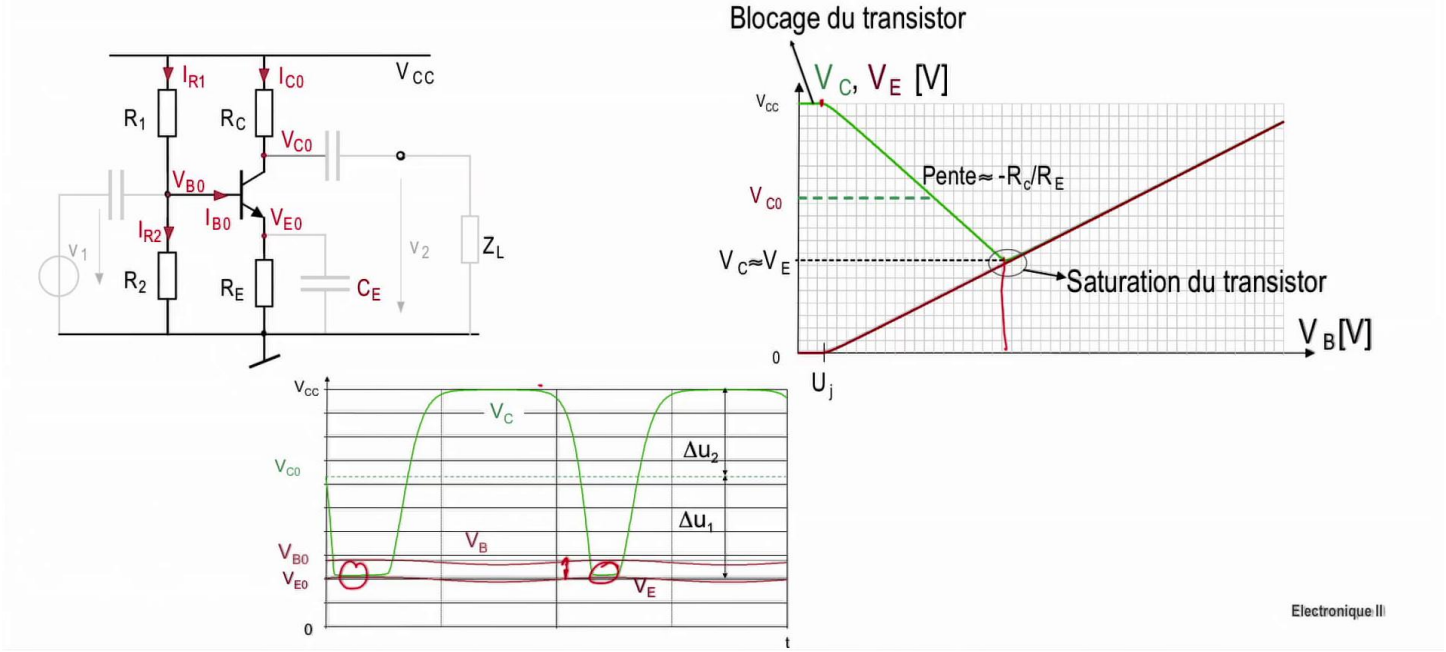
And this is the behavior of this transistor: I'll show you what's happens with, if I add a signal here which arying at the input so here I plug a signal, this is my editing, this is my DC analysis of my editing and there I took my editing and I have varied at a low frequency of course to prevent the capacities to do anything so I connected a voltage source here I did varied like that and I looked at the behavior of VC, I see that, then I applied a very low f requency signal on VB, I see that the same signal is on VE with a shift of UJ, this UJ which is between the 2 is shown there, it is between these two there. So what's interesting in there is that the voltage VC that I see here, I have voltage VC nonlinear because this VC when the transistor is off, he stuck to VCC. And when VC reaches VE, So you see when VC reaches VE is in those points, my transistor is saturated, the VCE is equal to 0 and we see these nonlinearities that occur, a low frequency sinusoidal voltage is applied, I insist on the word low frequency to say that it really is a change in the extremely low frequency to be seen as if it had been a DC variation and we seen that the signal that rises and falls like a sinusoidal gave a signal which is absolutely distorted, when transistor typed account, he blocked.

Notes

Summary

16m 27s

Point de fonctionnement/repos et Grands signaux



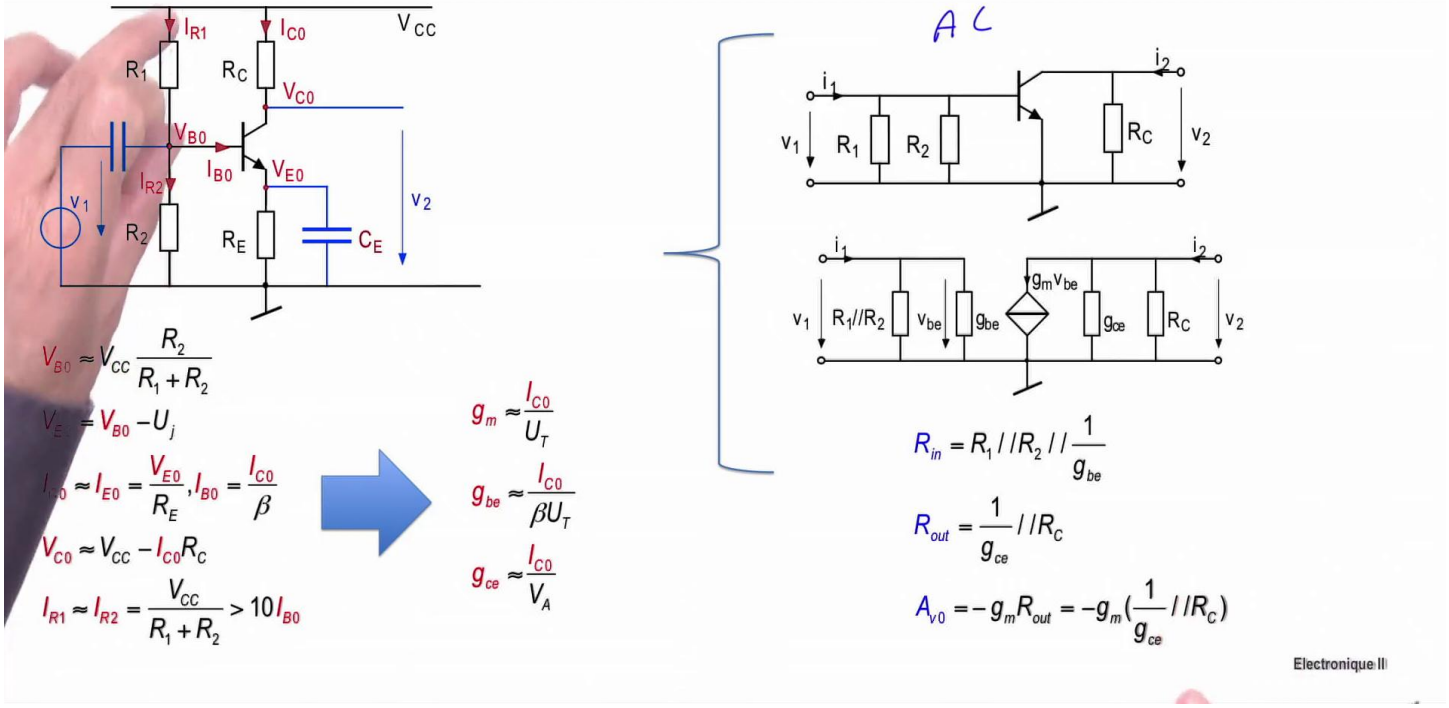
Here we found VCC that does not vary and when the transistor saturated, we saw the effect of saturation so we walked on this straight line and we put a VB variation which surpassed the dynamics of this. And here, I used the term: the dynamics. So I was putting a tension much larger so that my transistor saturates or blocks and that is what will define what we will call the dynamic. So this curve allows me to see what is my transistor operating range when it's linear and I can say that for such value equal to VB and this tension there, I have a linear area having a slope -RC / RE and it will give me what I'll call after the gain of this assembly with respect to a continuous signal as imposing upon entry and I do vary at low frequency.

Notes

Summary

18m 03s

Schéma petits signaux (AC)



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$$V_{C0} \approx V_{CC} - I_{C0}R_C$$

$$I_{R1} \approx I_{R2} = \frac{V_{CC}}{R_1+R_2} > 10 I_{B0}$$

$$g_m \approx \frac{I_{C0}}{U_T}$$

$$g_{be} \approx \frac{I_{C0}}{\beta U_T}$$

$$g_{ce} \approx \frac{I_{C0}}{V_A}$$

$$R_{in} = R_1 // R_2 // \frac{1}{g_{be}}$$

$$R_{out} = \frac{1}{g_{ce}} // R_C$$

$$A_{v0} = -g_m R_{out} = -g_m\left(\frac{1}{g_{ce}} // R_C\right)$$

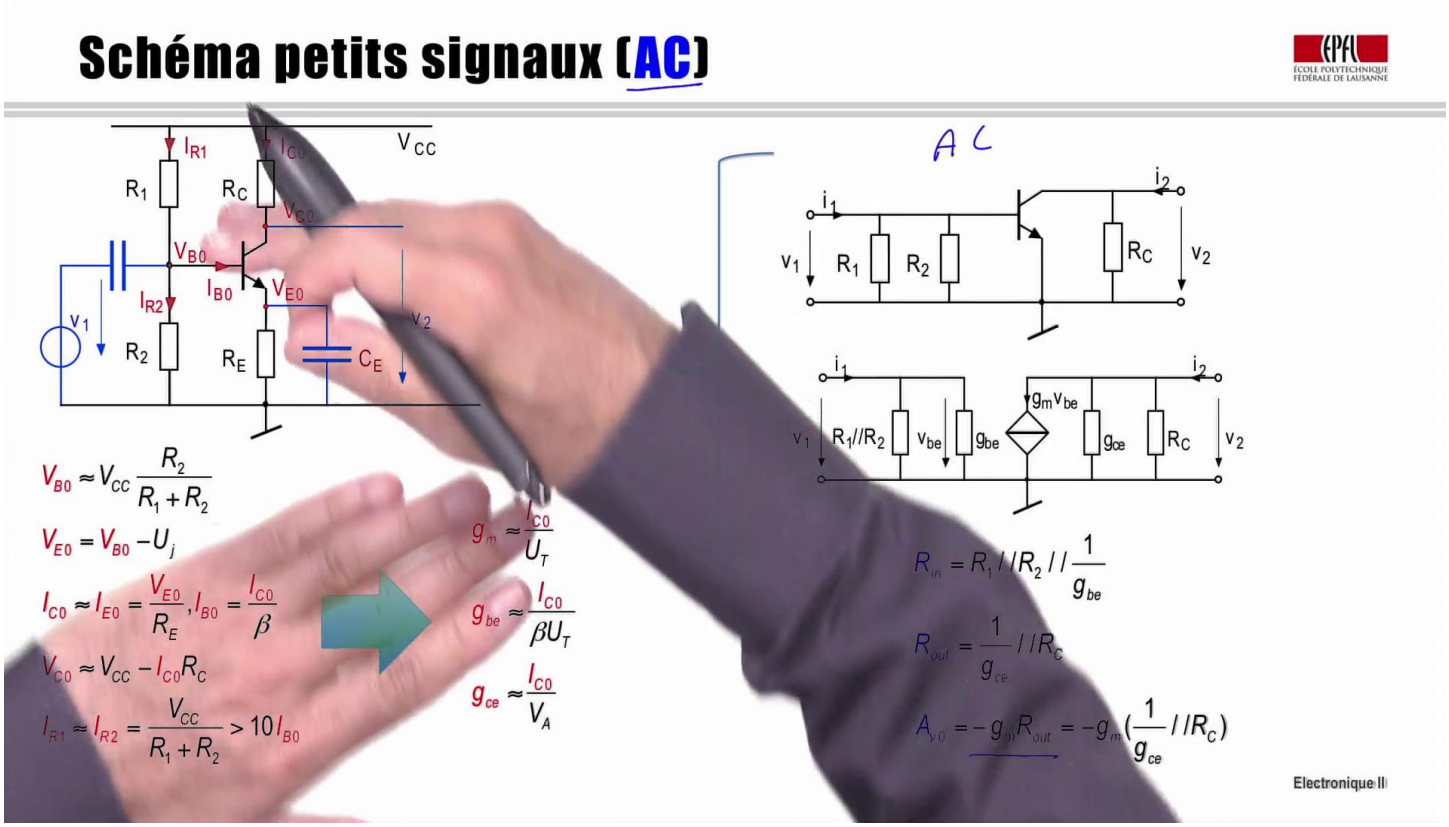
Electronique II

I continue the analysis of this assembly, I eliminated the resistance that I added here just so you do not put it back in parallel with RC otherwise if I said there must be considered RC that is in parallel with the impedance was there but then I have to put what is blue because I would like to analyze in AC what is happens with my assembly so I take a variable source in time having a frequency sufficiently high that this capacity is shorted-circuited and all this behaves as a high pass filter and that this also allows current to flow in this capacity I calculated adequately for it creates a short circuit here and I take this circuit and I do his AC model here. The AC model of this assembly, that is what we had learned before, so I short-circuit which is connected to ground, so the resistance RC comes here and watch the RE resistance once short-circuited by this capacity it will disappear. The two resistors R1 is in parallel with R2 because they brought VCC and was shorted-circuited and I keep my transistor, we agree that this is a symbolic representation in order to apply the AC model, otherwise you can remove this transistor and replace the model small signals we had studied before.

Notes

Summary

19m 06s



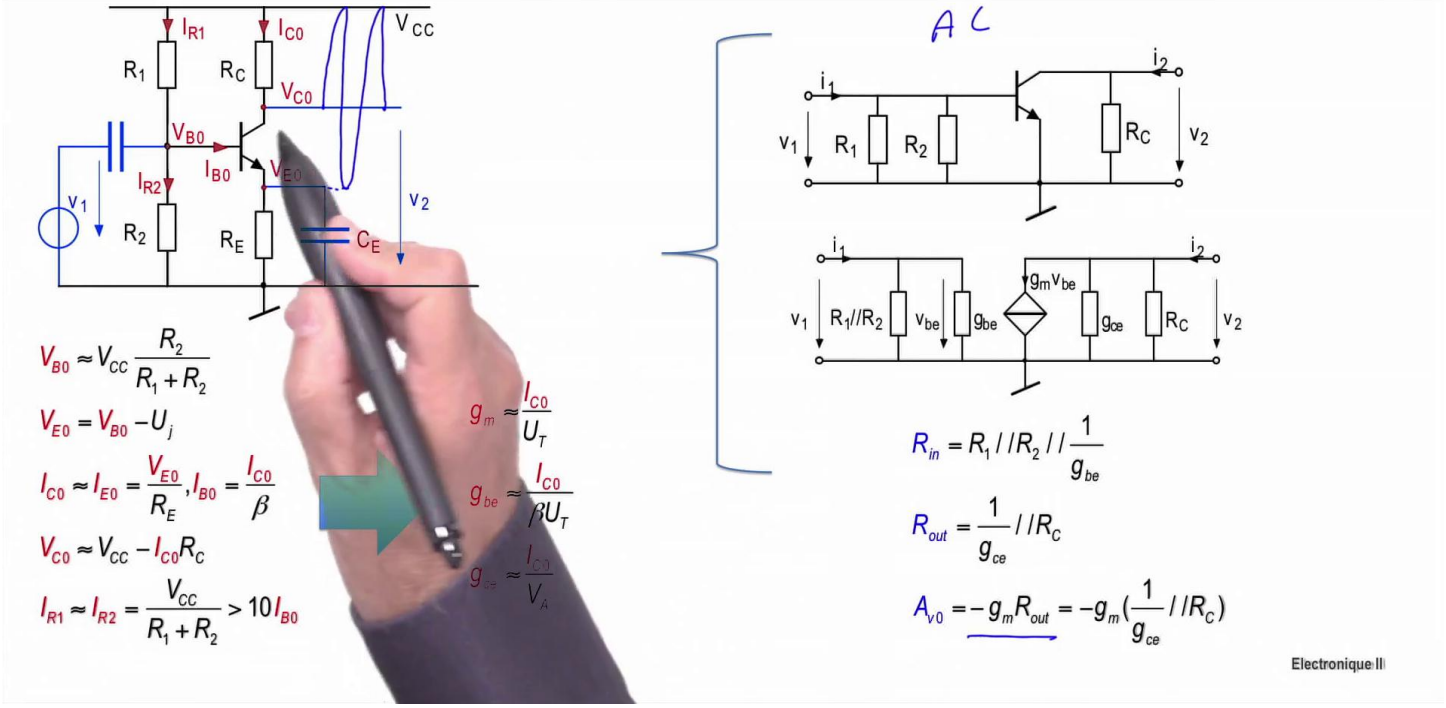
And the calculation here is a very simple calculation, it has been done before, it shows that I have a gain equal to -GM multiplied by the parallel of 1 / GCE parallel with RC. And the impedance seen at the input, it is the paralleling of these two resistors parallel with 1 / GBE and that is what is written here. Therefore the input impedance is known, the output impedance is known, and the voltage gain is known. So the fact of having added this capacity, it allowed me to fall on the gain expression that had been found for a common transmitter because well and truly your transmitter is in common, it has been connected to the ground and it has become in common between the input and the output. Look, with this capacity and found expression of the gain what we had to analyze a common emitter. So a common emitter after polarization needs this capability and this capacity will allow us then to impose a potential VE0 will remain fairly stable. This capacity, she is so great in his choice We shall study later how it is properly calculated, but this ability is so great and imposes a constant VE0 potential. So finally, your transistor, it will be stuck by the VCC voltage and VE0.

Notes

Summary

20m 28s

Schéma petits signaux (AC)



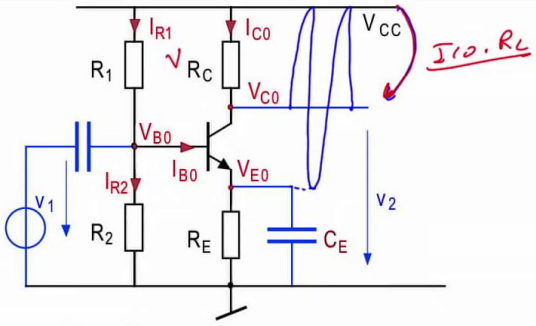
And there I come to the most important point of the transistor of use, is that we wanted him applying a variable voltage here and there find the exit and was presented and was told that there is a gain, but it is a gain that does not mean anything. If your signal is distorted, ie if your signal is which is the output which has a dynamic, this is the important word I would use which is within this range there, watching my 2 fingers my 2 fingers to see a DC voltage VCC so a direct voltage VE0 if we consider that C the capacity is infinite and the voltage VC here can rise there all your tension, it can rise up here And it will go down to here and that is the maximum Why ? Because if you bring it to go beyond that, your signal can not And if you ask him to go lower than VE0, your signal can not. So if you ask this question to someone, there is a ceiling and a floor and you want to make sure that there is something which is between the 2 having the maximum of dynamics, therefore the maximum opportunity to swing in, This person will tell you then choose VC0 In the middle of these 2. So if you set VC0 to VCC - VE0 / 2 you have answered the question that your signal dynamics is the greatest possible.

Notes

Summary

21m 54s

Schéma petits signaux (AC)



$I_{C0} \cdot R_C$

$$V_{B0} \approx V_{CC} \frac{R_2}{R_1 + R_2}$$

$$V_{E0} = V_{B0} - U_j$$

$$I_{C0} \approx I_{E0} = \frac{V_{E0}}{R_E}, I_{B0} = \frac{I_{C0}}{\beta}$$

$$V_{C0} \approx V_{CC} - I_{C0} R_C$$

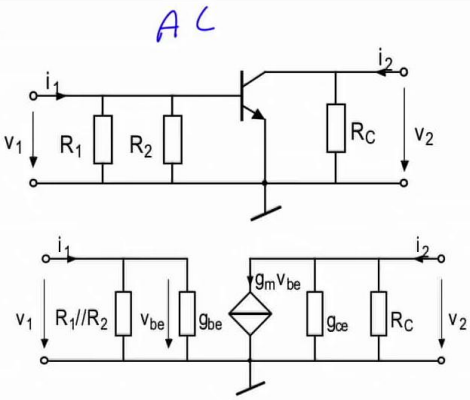
$$I_{R1} \approx I_{R2} = \frac{V_{CC}}{R_1 + R_2} > 10 I_{B0}$$

$$g_m \approx \frac{I_{C0}}{U_T}$$

$$g_{be} \approx \frac{I_{C0}}{\beta U_T}$$

$$g_{ce} \approx \frac{I_{C0}}{V_A}$$

AC



$$R_{in} = R_1 // R_2 // \frac{1}{g_{be}}$$

$$R_{out} = \frac{1}{g_{ce}} // R_C$$

$$A_{v0} = -g_m R_{out} = -g_m \left(\frac{1}{g_{ce}} // R_C\right) = -\frac{I_{C0} R_C}{U_T}$$

$= -\frac{V_{RC}}{U_T}$

Electronique II

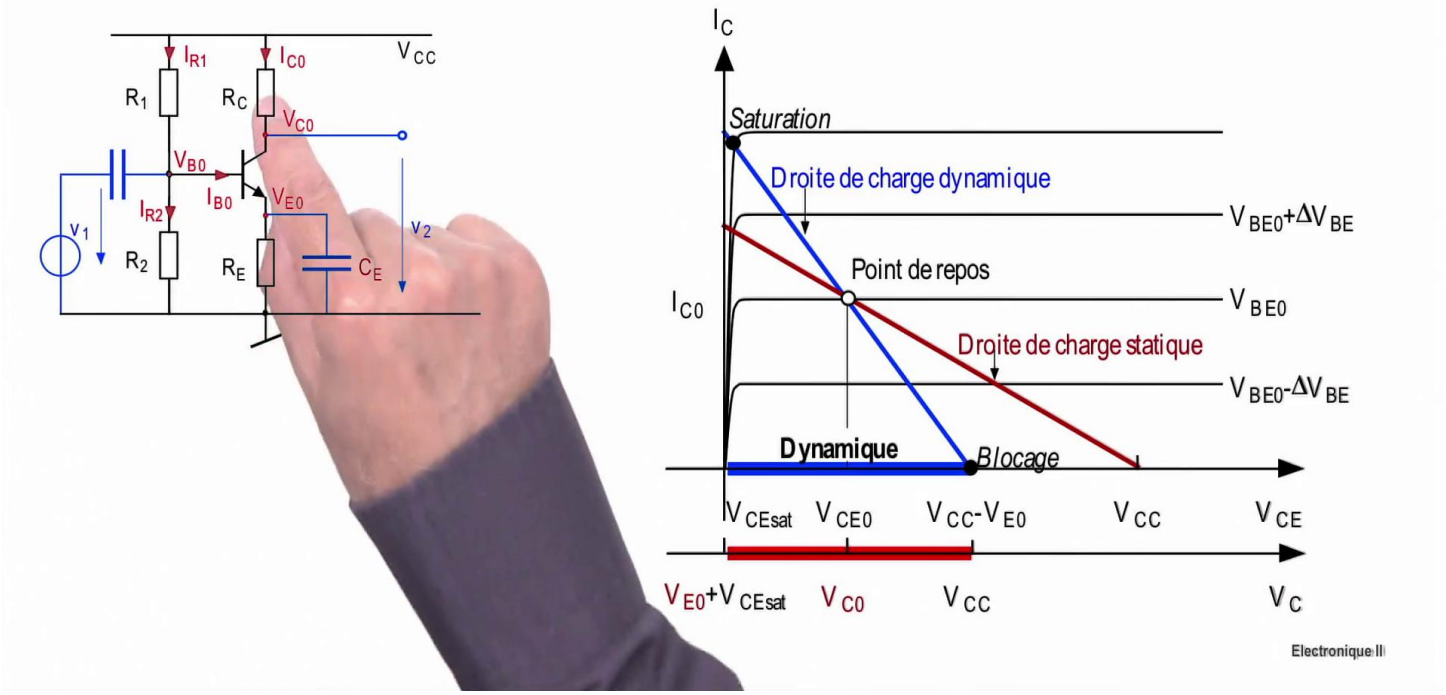
And that is the most important parameter in the design, this is the dynamic, this is not the gain, because VC0 tension, I'll write it elsewhere, the VC0 tension, this tension from here to there in DC, I should do it in red, this tension from here to there in DC what is it? This is IC0 multiplied by RC. So this voltage I0 x RC. look I'll write something in the gain here I'll replace GM with its value GM with its value or rather I will write here GM is worth less IC0 divided by UT Multiplied by R out and R out in this case is RC here if we neglect the 1 / GCE therefore multiplied by RC. So that, we have neglected this it gives this value IC0 RC well that's what I wrote here. So I can write the gain very well as being less, we'll call it HRV minus VRC divided by UT. And that HRV is the voltage from here to there, DC and it is this tension then that generally you had to choose equals VC0 - VE0 for that and it is the same, therefore as soon as the dynamics have been chosen, we have imposed the gain as well. So this is the The most important that a circuit designer should pay attention, is choosing the operating point such that VC0 is In the middle of that beach And once we chose this, this is one ignores it and falls on the fact that the gain depends on this dynamic too.

Notes

Summary

23m 23s

Droites de charge statique et dynamique



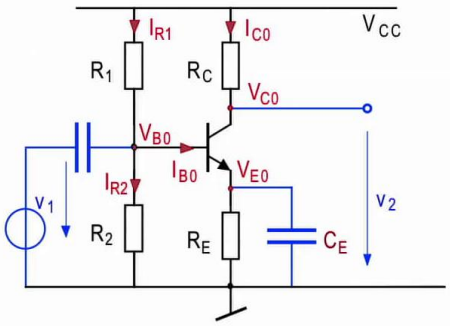
I would like to comment on the so-called load lines, straight with S because there are two lines of loads. There is the charge line Which is due to the fact that in DC, capacities are involved. That's what we did when we put a DC voltage source here. If you vary the tension there and you watch what happens on the voltage VC0, So I bring this voltage VC, you'll see this line, this line corresponds to the variation of current with respect, I hear the voltage VC with respect to the current IC. By increasing the voltage VB, you increase IC and you will fall or raise this potential and we find what is called the line of static charge. do not forget that at that time The resistance RE will act because this capacitance has no effect it is as if this capability does not exist. And if you look at the slope of this straight line it will depend on RC and RE at the same time, but if you put an AC signal having a frequency Which causes this capacitance to be short-circuited, so your RE resistance is short-circuited, you end up with your issuer that is pulled to ground and the load line will depend solely on RC, you straighten your static straight.

Notes

Summary

25m 20s

Droites de charge statique et dynamique

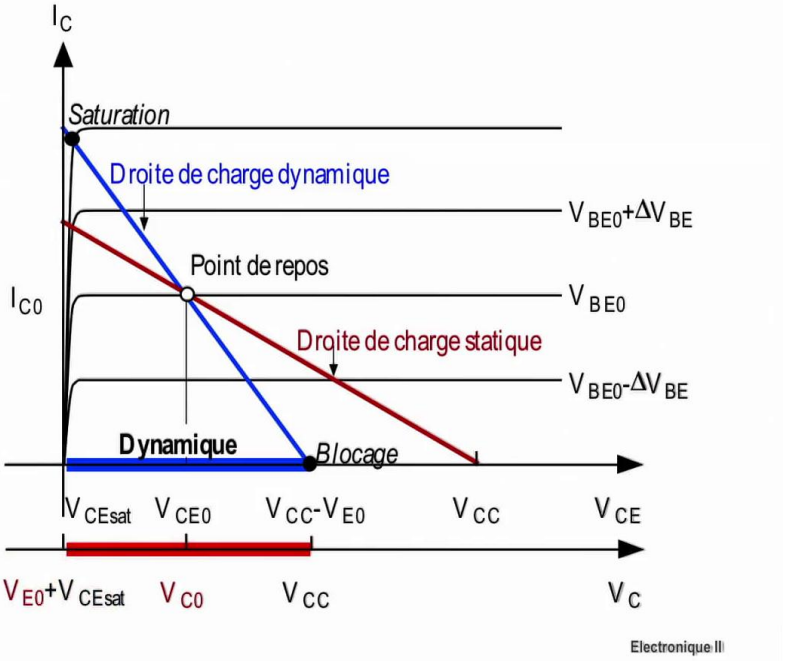


Droite de charge statique:

$$I_C = \frac{V_{CC}-V_{CE}}{R_C+R_E}, \quad \text{Pente} = \frac{1}{R_C+R_E}$$

Droite de charge Dynamique:

$$\text{Pente} = \frac{1}{R_C}, \quad \text{Dynamique} = V_{CC}-V_{E0}-V_{CEsat}$$



Electronique II

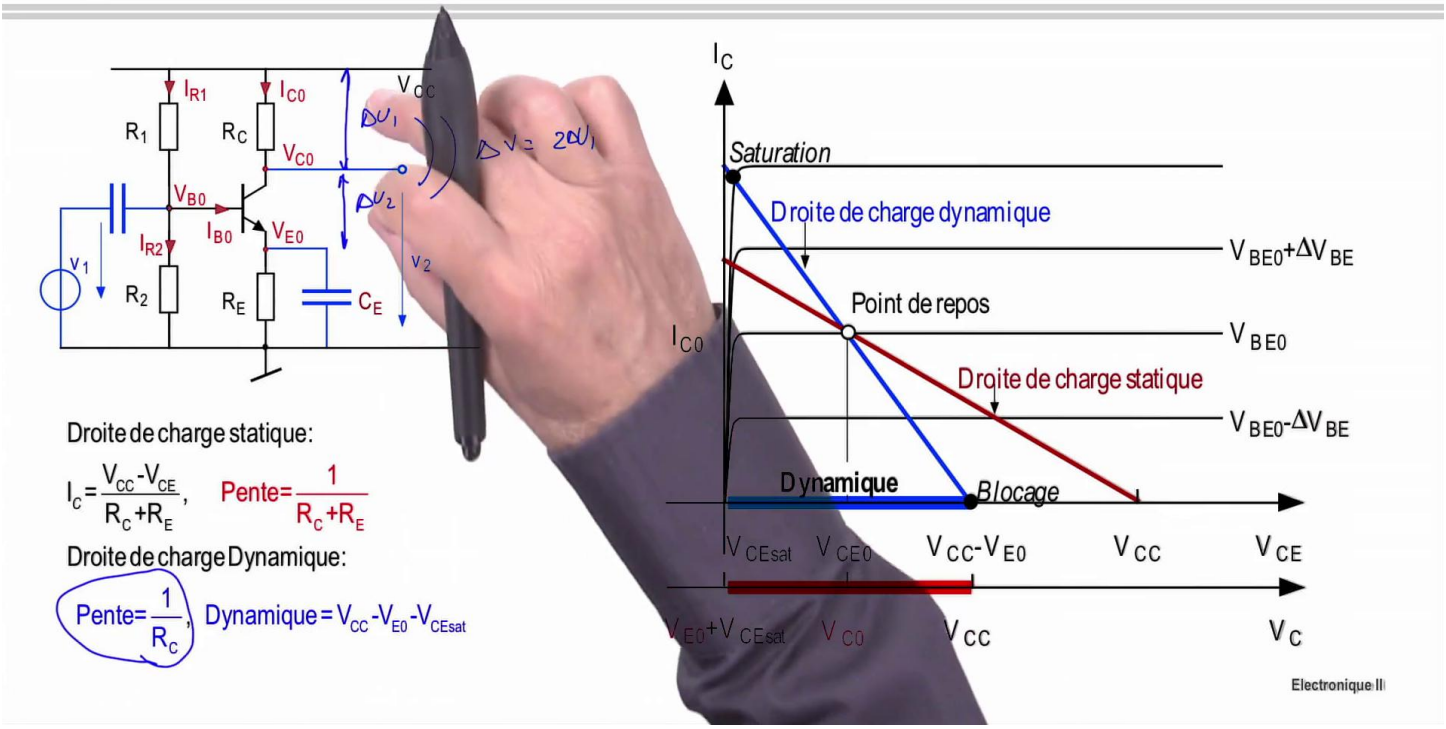
The fact of removing RE connected to the right then Statically speaking to a DC signal, the fact of bringing an AC signal, suddenly your gain increases, that's what we had seen earlier and this is what makes the load line it will increase and this load line this is actually the speech I had done before, it will depend on this VE0 tension and this voltage VCC and its mid-point it must be VCC0 which is also the intersection of 2 straight because on the rest VCC0 does not vary it is dynamic or static, we will see here the VC0. But once you put an AC signal, we see the disappearance of RE and the gain and increased load of the line straightens it will give us what is called dynamic load line and the point of intersection of the lines 2 corresponds to this potential VC0 of this assembly. So this choice VC0 is absolutely important, must be distinguished Use AC and DC and it is necessary to know that when using this kind of editing which depends on a signal AC and we gain by the fact that it removes and boost gain and it is necessary to choose adequately the potential VC0. And the summary of what I just said is there. Static load line does not see the effect of the capacity that allows for RC and RE, this is what we see here.

Notes

Summary

26m 54s

Droites de charge statique et dynamique



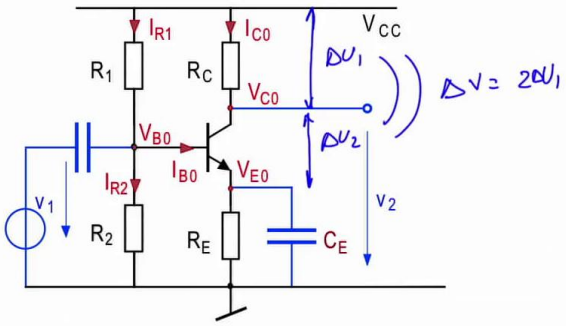
The right dynamic load see especially the resistance RC because RE it's do short-circuit and the dynamics, that is, all that part from there to there or from here to there. If by chance, someone has chosen VC0 - VE0, very close to each other, your transistor will saturate it before it crashes. So why make a transistor saturates before it blocks? So your signal at the output is already distorted by the saturation. So the best choice is to have saturation, That beach and that beach is the same. and we called dynamic whole excursion, that for which your signal is not distorted. So it will take, if delta U1 is from here to there Delta and U2 is from here to there, if you have delta delta U1 equal to U2, you have a dynamic that is equal in Delta V1 to exit 2 times delta delta U1 or U2 or... if by chance you have a delta U1 lower than delta U2, you choose the lowest, you multiplied it by 2 and you say it's my dynamic, because it is useless to...

Notes

Summary

28m 29s

Droites de charge statique et dynamique

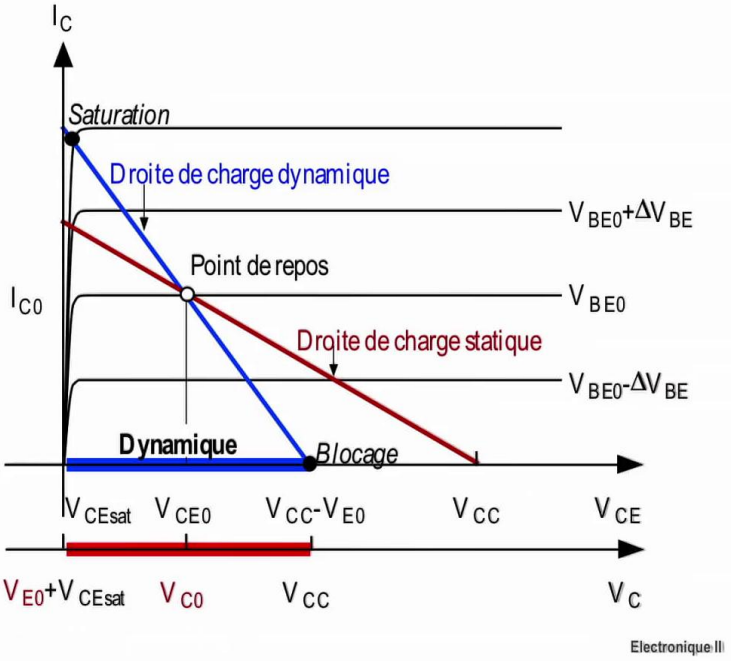


Droite de charge statique:

$I_C = \frac{V_{CC}-V_{CE}}{R_C+R_E}$, Pente $= \frac{1}{R_C+R_E}$

Droite de charge Dynamique:

Pente $= \frac{1}{R_C}$, Dynamique $= V_{CC}-V_{E0}-V_{CEsat}$ $(=0)$



Electronique II

to speak of a signal at the output if it is not linear, therefore we choose the value the lowest of these 2 and multiplied by a factor of 2 and we say the dynamics is equal to that or in other words if you take this right then and you're good at designing, you choose this, this, absolutely equal to this and your dynamics will be what I have drawn in blue here and at that time If VCEsat is equal to 0 therefore it is considered: your momentum is equal to all this VCC - VE0. And that's really the most important thing when we doing circuit design is to come to respect and to increase the signal dynamics at the output.

Notes

Summary

29m 57s

Résumé

Finally, I take my amplifier with active load, we have already analyzed, you know it, the gain, I have already calculated it before and I wrote it I have already calculated it before and I wrote it down. I have already calculated it before and I wrote it so what is the dynamic here? The dynamic here is maximum. Why ? Because it will depend on the saturation of this and saturation of this. So, just now, we had to lose a certain amount when there was resistance in the transmitter. There I can normally go up to VCC and down to 0. And this potential here, he is determined by the stage which follows, so if the next floor does not block this tour, we have what we call a "rail to rail" because this is feed rails and is said to be a rail-to-rail assembly because it is capable of Change the potential up to VCC If the saturation voltage is close to 0 and drops down to 0 and dynamics of active load mounting is much higher Than the resistance mounting dynamics for the same voltage levels VCC and for the same power. I have just finished the presentation of simple common emitter with resistance concrete, passive and active we address the most important problem of designing which is called the momentum.

Notes

Summary

30m 38s

Amplificateur émetteur commun à charge active

- Dynamique maximale:

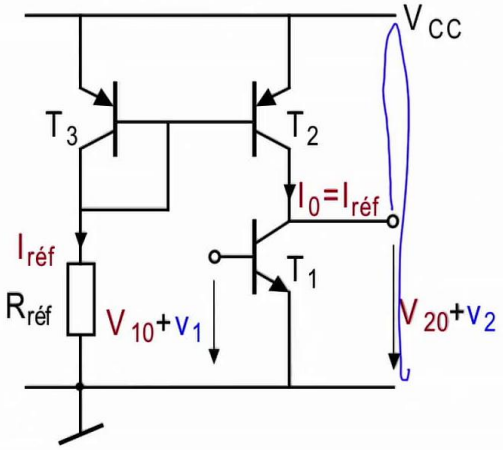
✓ V_{CC}-V_{CEsat1}-V_{CEsat2}

- Gain intrinsèque maximal:

✓ $$A_{v0} = -g_{m1}\left(\frac{1}{g_{ce1}} // \frac{1}{g_{ce1}}\right) = -\frac{g_{m1}}{g_{ce1}+g_{ce2}}$$

$$R_{in} = \frac{1}{g_{be1}}$$

$$R_{out} = \frac{1}{g_{ce1}+g_{ce2}}$$



Electronique II

I insist on this aspect and someone who understood what is a dynamic assembly, will understand very well that this is the most important aspect when you make a circuit design, it's to get to realize the maximum dynamic you will see later that even get a mounting performance quite high, it's thanks to the response, at the output that is get to achieve maximum dynamic also answer your question that the assembly has an optimized and maximum performance.

Notes

Summary

32m 13s