ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

6.3- Exemple

Structure d'un Amplificateur Opérationnel

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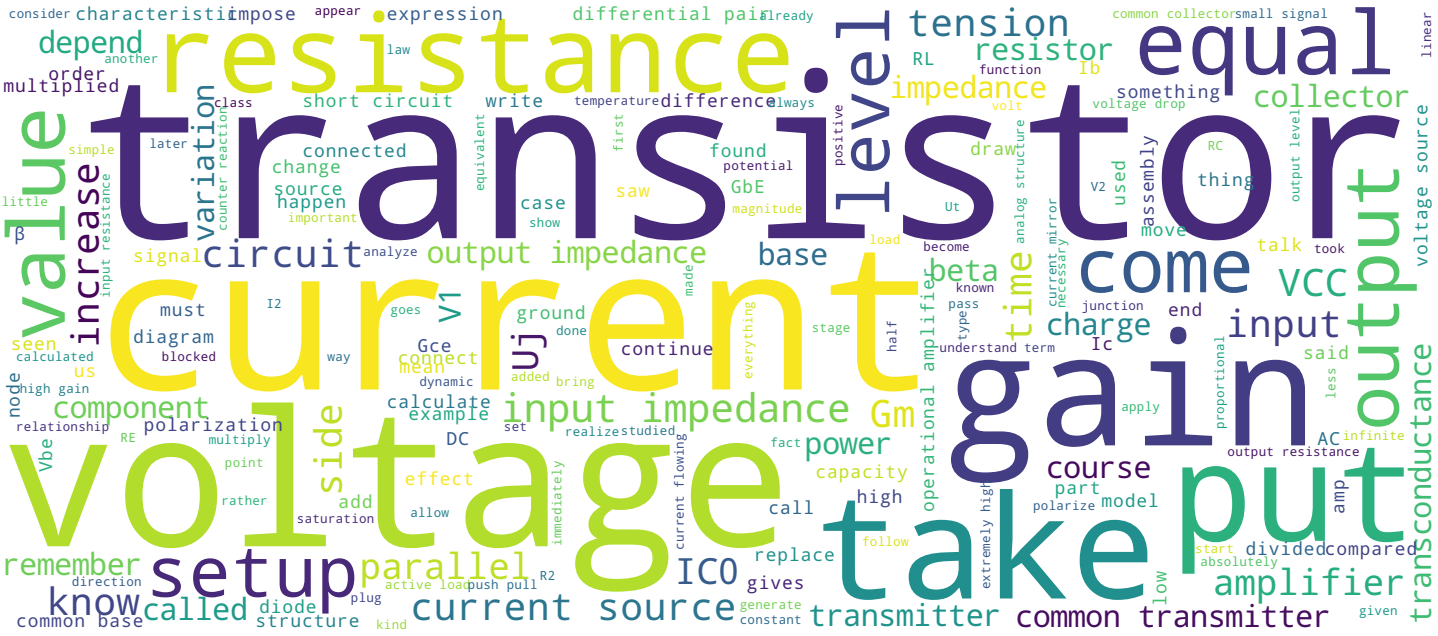
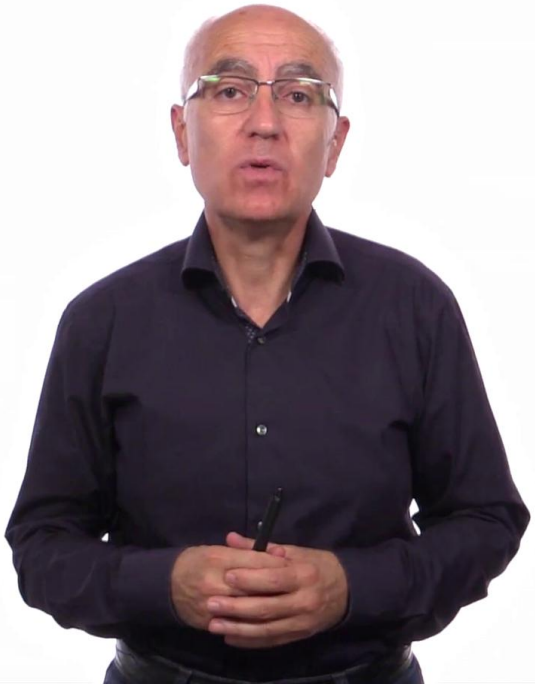


Video

EPFL

Résumé



- Introduction
- Structures analogiques en cascade
- Analyse et estimations des paramètres

Electronique II

Well, compared to what we just saw in the video before, I promised that we will now move on to the use of these functions and analog structures. And we will build together an operational amplifier, which is made with three levels that follow each other.

Notes

Summary

0m 05s

Amplificateur Opérationnel Idéal

- Gain idéal:

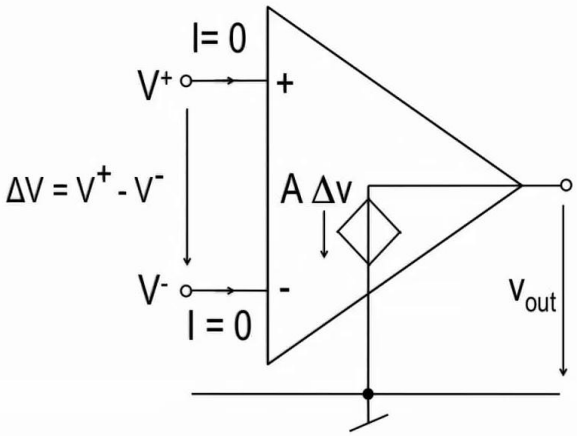
$$A = \infty$$

- Résistance d'entrée:

$$R_{in} = \infty$$

- Résistance de sortie:

$$R_{out} = 0$$



Electronique II

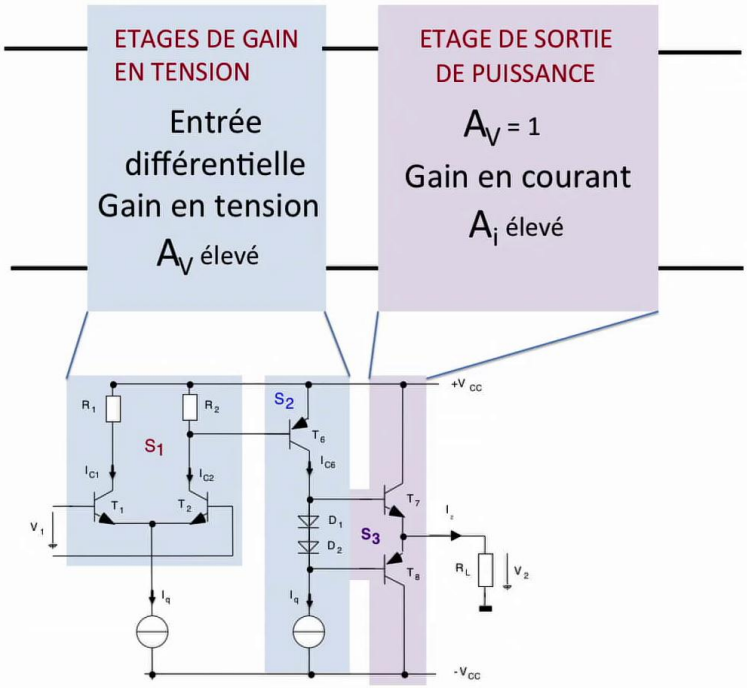
Before starting, see what we will do, I'd like to remind you what is an operational amplifier. So, an operational amplifier, we gave it these characteristics that you see here. We would like that, ideally, we have an infinite gain A or a gain in any case very, very high. We wish that there is no current entering in the positive and negative strip if not, we will have an extremely low current here. So this comes down to say the input impedance is infinite. We wish to draw from it an infinite current without disrupting this voltage. That is to say that the series resistance, we have seen here, is zero. With these three characteristics, I can say, It is necessary to constitute in this black box containing a + input, an input -, an output voltage, I should reach a very large gain. I should make sure that the entries have very high impedances, and the output has a very low impedance. And let's go with the analysis of what is inside.

Notes

Summary

0m 23s

Etages d'un amplificateur opérationnel



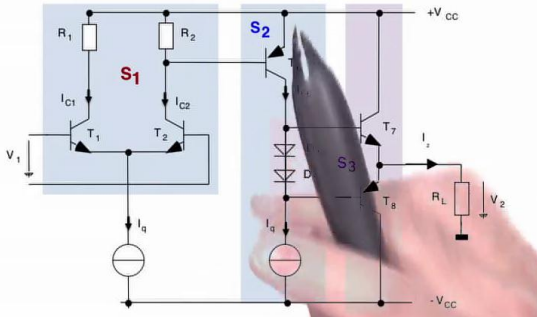
If I turn into levels, to an operational amplifier, I could say, since I have to make a level that makes the gain, then let's do: levels may be with "s", level without "s", there will be a single level that makes an infinite gain or one level, or 2 or 3 levels, which make a voltage gain infinite but which also possess one differential input because I want to make the counter-reaction- with the negative terminal, and at the same time, I would like that the current who passes, is very, very low. We'll have as I make an output level, and this output level should not be contributing to the gain and, in any case, have a gain to the very high current, that is to say, it must have a very low input impedance with an output current which will be great. If you look at these colors that I put there, and you will see that I used two levels to realize what I call the gain level, that's why there is the "s" here and a level to make the output stage. And we will take this structure there and start to study it far and wide, and then I'll ask you to do this exercise and calculate the gain with numbers after this video.

Notes

Summary

1m 40s

Structures à trois étages et une polarisation



S1: étage d'entrée formé d'une Paire Différentielle(P-D) avec une charge passive avec sortie asymétrique.

S2: étage intermédiaire Emetteur Commun (E-C) qui génère un grand gain en tension grâce à une charge active.

S3: étage de sortie push-pull de grande impédance d'entrée et de faible impédance de sortie avec un gain en tension unitaire, mais un gain en courant $\beta >> 1$ capable de fournir du courant à la charge RL.

Electronique II

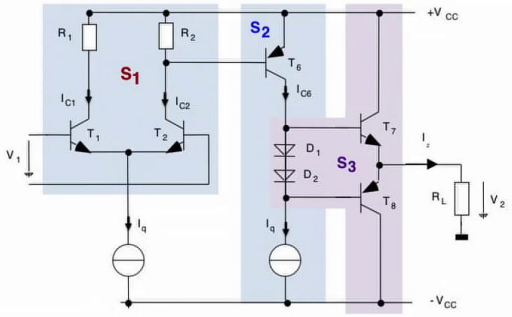
Take this and look at what I noticed. You remember, I called it "analog structure." So "S" as Structure, where I S1, S2, S3, I have 3 structures here. I will read what I have noticed in the face: I called S1: S1 is an input level formed by a differential pair, so the floor is formed by a differential pair with a passive load and an unbalanced output. Why asymmetrical? Because if you remember, a differential pair, I can go out there and there at a time, but then I decided to go out from only one side so I have an unilateral output, just to read the voltage which is from that side there. The structure S2 is an intermediate floor as a Common type transmitter, which must have a large gain why I did not notice it here and although I have not spoken of gain here, because if you noticed, of how to incorporate this thing or to carry out this circuit, I opted to put a passive resistance, So usually, when you have a passive resistance here the gain is relatively low, that's on one side... On the other side, the fact to having plugged this level here I am condemned to see the input impedance from this level.

Notes

Summary

3m 00s

Structures à trois étages et une polarisation



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Electronique II

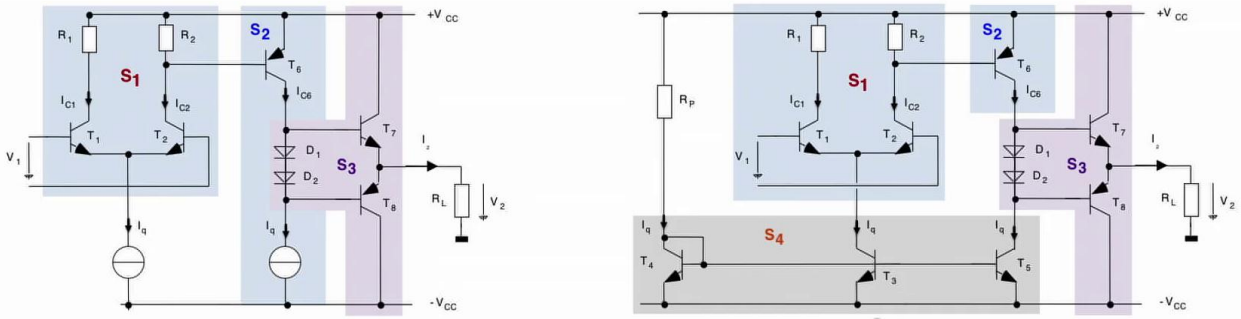
The input impedance of this stage is 1/GbE in transistor which is usually not biger than that, so it is useless to put an active load here I'll be condemned to use a filler here passive in nature because I break the gain with the input impedance that I see here. If we take this, and we look at the level to the end, I would see that S2 has a large gain through an active load because I have put an infinite resistance. I took the collector of this transistor, I disregard these two diodes, because these two diodes in terms of AC, it is practically two series resistors, are the differential resistances of the two diodes that we can neglected here and in series with the huge impedance, this huge impedance is a current source therefore dull in resistance is infinite resistance. Of course, this level here should see an input impedance, here, which is very, very big otherwise I risk breaking the gain.. And I finished with the S3 structure which is here is a "push/pull" assembly linearized with two diodes: D1 and D2.

Notes

Summary

4m 21s

Structures à trois étages et une polarisation



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S4: polarisation avec un miroir de courant à sorties multiples. T4 monté en diode en est l'entrée, T3 et T5 en sont les sorties qui se comportent comme des sources de courant constant Iq. T3 polarise la P-D et T5 est la charge active de l'E-C.

Electronique II

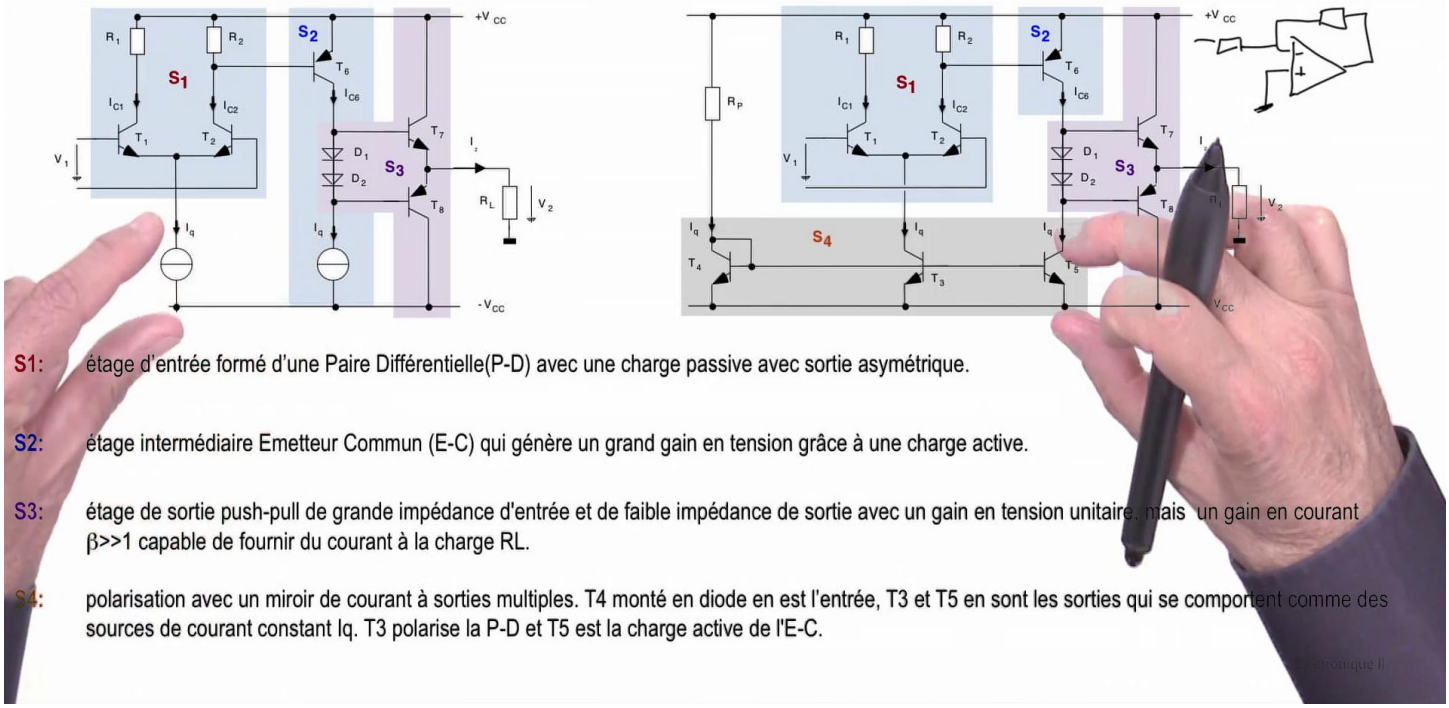
So I read: output level push/pull of high input impedance, so I'm supposed to have a high input impedance here and low output impedance, which is normal, there, I have a low output impedance Because I exit on the transmitters and if you remember, the impedance of a transmitter is low with unit voltage gain, so it is a gain equal to 1 but a very high beta current gain, very often, instead of a single transistor, here and here, we put</ i> Darlington transistors to use beta 1 x beta 2 of two transistors, that allows us to have extremely high beta. So that is capable of providing a current in the load RL taking account of a weak current that goes here much current fgoes from there, Remember that the output current goes like this. So, I take very little control current I multiply by beta and the majority of the current I draw it by there in the or from the mass, to the other transistor. So there are two stories here, they are current sources which are not executed with transistors. Then I will take the complete digram that will be the next: that's the conceptual diagram, that's the full diagram. The difference is that I replaced active charges by active charges diagrams that is to say, I take a current mirror, I call it S4, and I used here.

Notes

Summary

5m 36s

Structures à trois étages et une polarisation



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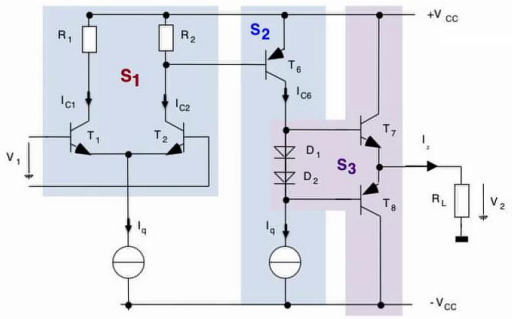
to polarize my differential loss and there to realize an active charge Look at the difference of the same current mirror, which takes the same polarization and that generates the same bias current. This transistor one it is supposed to lead us to have a voltage variation this transistor there is not caused to have a voltage variation because if you take this operational amplifier and if you decide that, your amp is something who is going to be like that, I'll put it as follower assembly or rather in inverter. There is one input of the positive terminal which is connected to ground, which means that there is a inputs connected here to ground and when it connected to ground, the voltage drop of 0.7 volts is fed directly on that node there, that node there is stable because it has a stable voltage here and any small variation here it is due to the output conductance when I have a common mode which can move or imperfections of my operational amplifier. I wanted to say that this transistor there, it plays the role of a charge. On the other hand, this transistor here, plays the role of a current source for biasing DC current.

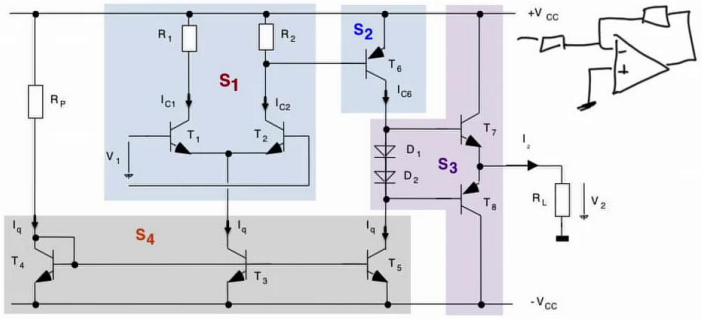
Notes

Summary

7m 05s

Structures à trois étages et une polarisation





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Electronique II

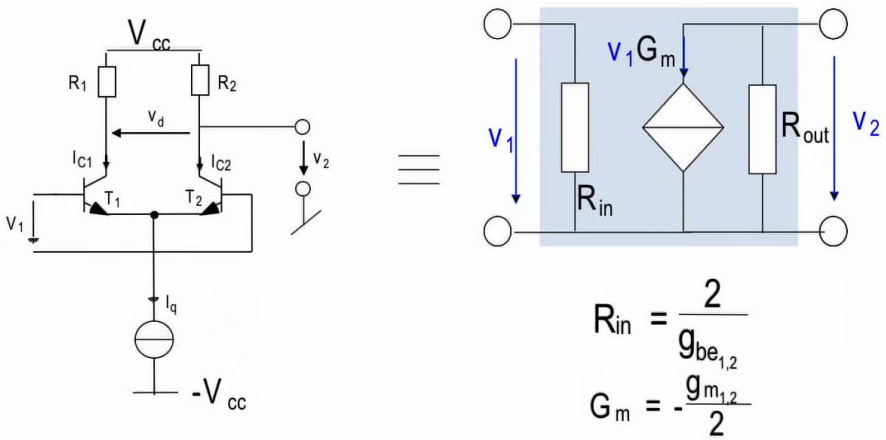
And the two are part of a mirror of current, where the single current, and to generate one and the other comes from the diode or the transistor diode-connected and a stabilized voltage source that would have to feed our "amp" and a bias resistor. So we have our four structures: a transconductance, a second transconductance there I am saying the name of the functions which were used in the output stage and one bias and an active load and the 2 are derived from a simple current mirror, And then, we went through what we just saw in the previous video concerning functions, and they are now in the form of analog structure, and their link with the functionality in an amplifier.

Notes

Summary

8m 23s

Analyse de l'étage d'entrée



$$R_{in} = \frac{2}{g_{be_{1,2}}}$$

$$G_m = -\frac{g_{m_{1,2}}}{2}$$

$$R_{out} = R_2 // (1/g_{ce2}) \approx R_2$$

Electronique II

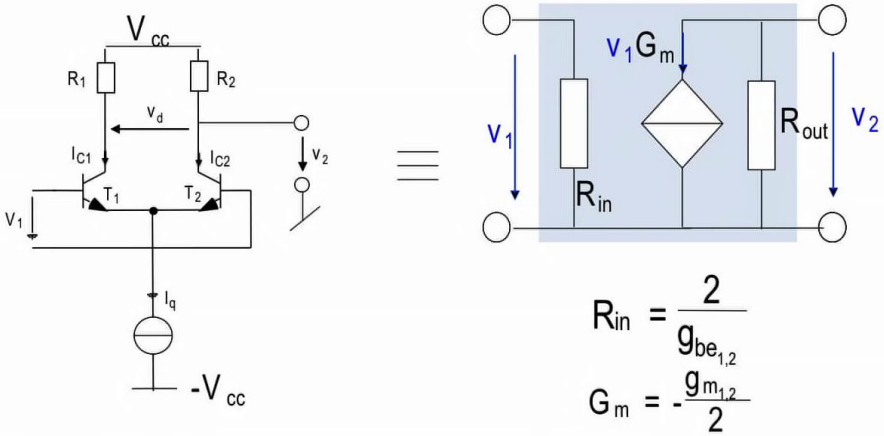
I will go level by level, and I'll analyze what I get with modeling, that we studied in the course. So we studied that, when I am dealing with a differential pair, I take my differential pair and I'll watch the equivalent of AC. The source of the current, here will disappear. The equivalent diagram of a differential pair, I refer you to the course on differential pair, and just This has an input impedance, an output impedance, a controlled current source with a transconductance. The input impedance it had been calculated, it is 2 / GbE, either one or the other, because it is the same GbE, at rest, we have the Iq current that will pass in half here, and half there. So we will be with the half current in one and in the other, and the voltage V1 is distributed between a junction and a second junction, and when a junction sees a high voltage, the other sees a lower voltage, which brings me immediately to understand that is as a common emitter, apart from that the impedance she finds multiplied by a factor of 2: the input impedance. The transconductance is the half of each of the transconductances, And the output impedance, then you have to ask the question</ i> from this impedance.

Notes

Summary

9m 13s

Analyse de l'étage d'entrée



$$R_{in} = \frac{2}{g_{be_{1,2}}}$$

$$G_m = -\frac{g_{m_{1,2}}}{2}$$

$$R_{out} = R_2 // (1/g_{ce2}) \approx R_2$$

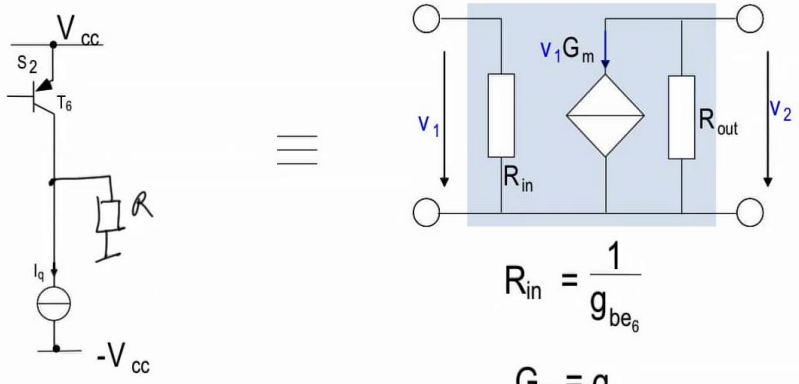
If that node there corresponds to a virtual ground, because if there is a common mode input, there is a voltage drop here DC, which requires a fixed potential this is where we see that I have 1 on Gce of this transistor here because I go out there on that node which come in parallel with the power supply, which goes back to the resistance R2 and in parallel with 1/Gce2. And often 1/Gce is high enough, compared to the load resistance so I can approximate it by R2. So I just took my differential pair and what we took as a model, I replaced the AC settings with the values that we have found. That I now possess a summary of what is my differential pair I put aside. I will continue with the next floor. It's very important this way. So I will not look at the whole of my operational amplifier, I divides it into each analog structure. The structure, I know its characteristics. I know it's his function, thanks to what I've synthesized and the values that are in there will depend of my bias currents that I have chosen which are inside.

Notes

Summary

10m 44s

Gain en tension: Emetteur commun



$$R_{in} = \frac{1}{g_{be_6}}$$

$$G_m = g_{m_6}$$

$$R_{out} = (1/g_{ce_6}) // (1/g_{ce_5}) // R$$

Electronique II

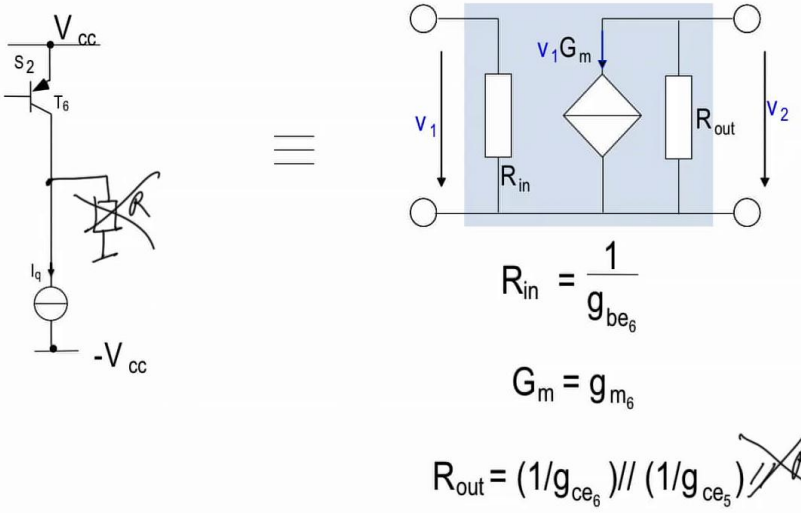
This is the second level. The second level is a transconductance again. the Structure 2, it is a common transmitter with an active load, the model of the transistor, I know, the input impedance, is that I see there, 1/Gbe of this transistor. The transconductance is Gm, the gain is Gm x R out and the R out here, you remember, instead of the current source, we had a transistor, so that's why it's 1/Gce6, parallel with 1/Gce5, because this transistor was the transistor 5. So I write the three parameters and I have everything that's necessary, gain is Gm X R of this setup. And that's pretty high, it will bring me a very high gain. At the moment I have not connected what would come after. If by chance, I just take the differential pair we saw before, and this level here, I already have the two gain levels. The product of two level gains gives me the gain level, provided that I do not come to break the gain here. If by chance we plug here any low resistance, look, it will come in parallel here. I call it R, and come here. So if this resistance is low, that's it, you've broken all the resistance R out of this setup and if you broke it, it is because of this setup here that generates the essential of the high gain.

Notes

Summary

12m 00s

Gain en tension: Emetteur commun



$$R_{in} = \frac{1}{g_{be_6}}$$

$$G_m = g_{m_6}$$

$$R_{out} = (1/g_{ce_6}) // (1/g_{ce_5})$$

$A_v = -g_{m6} \cdot R_{out}$

Electronique II

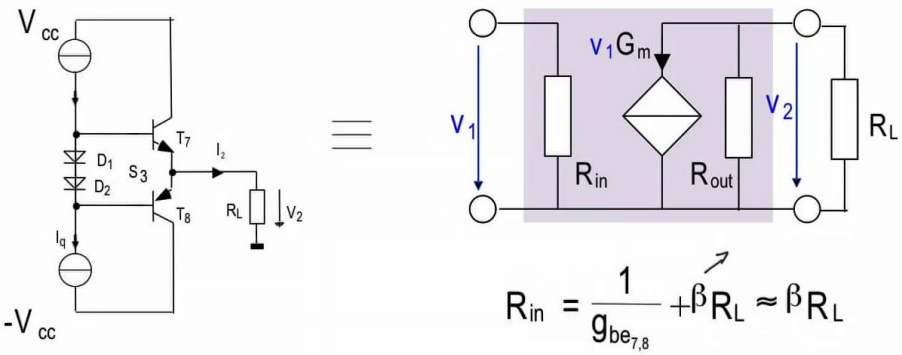
So if we take this low-resistance you will end up with R out equal to it, so the gain of this stage is: -Gm6 multiplied by the R out resistance of this level here. And there it is, if R out is low, I degrade the gain, and what I wanted to do, that is to get a very high gain, well I do not get it, because I degraded it because of this. So this is something I could not do and I connect a level here, the one which comes here, this level which will come here, should at all costs have an extremely high resistance here because it will come in parallel with this, I would not degrade the value I got here.

Notes

Summary

13m 39s

Etage de sortie



$$R_{in} = \frac{1}{g_{be_{7,8}}} + \beta R_L \approx \beta R_L$$

$$G_m \approx - g_{m_{7/8}}$$

$$R_{out} = \frac{1}{g_{m_{7,8}}} + \frac{(1/g_{ce_6}) // (1/g_{ce_5})}{\beta} \approx \frac{1}{g_{m_{7,8}}}$$

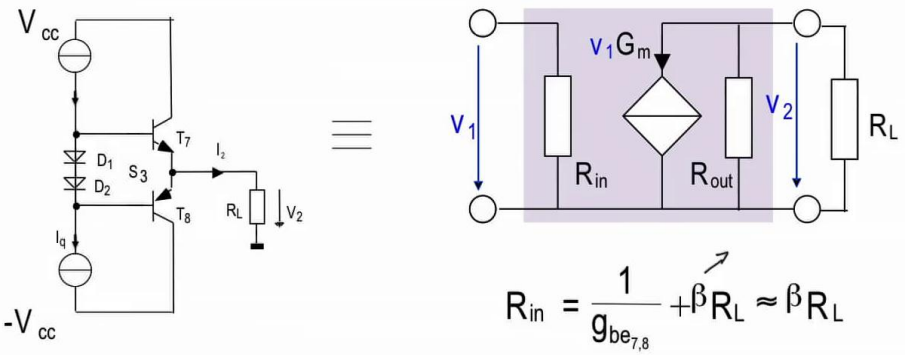
That's why I opted to take an output level. Hence the need for this output level when I plug on this side. Well, what I see on this side here, is the input impedance of a push / pull setup</ i> which is like the common collector, and its impedance that I see here is 1 / GbE + Beta X RL, So it depends on RL, it also depends on beta. For example, why we put Darlingtons here, instead of these two, we put Darlingtons so as to greatly increase the beta, because when we increase the beta, look at R in, it is more dominated by this factor here, this beta X RL. So often in our designs we put very high betas. The RL, it depends on the user. It is the resistance that you will connect by yourself when you use your "amp", if it is an audio amplifier and you put here a low-resistance of a few ohms, know that this level here, if it doesn't have a very high beta, it may decrease the gain. And generally thanks to the counter-reaction, we improve all this thanks to the gain in open loop of the set. That said, it is the overall pattern, or rather the model of my setup</ i> as we studied it, We know the input and output impedances, and we know that the output resistance is approximately 1 / Gm since that the gain will be Gm divided by the 1 / Gm.

Notes

Summary

14m 27s

Etage de sortie



$$R_{in} = \frac{1}{g_{be_{7,8}}} + \beta R_L \approx \beta R_L$$

$$G_m \approx - g_{m_{7/8}}$$

$$R_{out} = \frac{1}{g_{m_{7,8}}} + \frac{(1/g_{ce_6}) // (1/g_{ce_5})}{\beta} \approx \frac{1}{g_{m_{7,8}}}$$

Electronique II

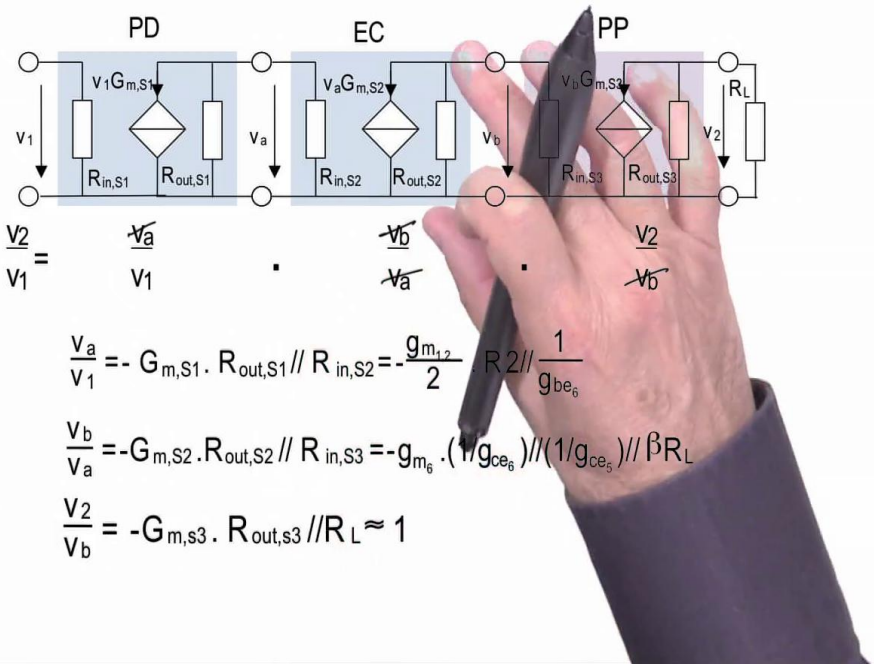
Look, this over this equals 1, so we end up with a diagram that will give us a voltage follower, where a gain equals 1. So I now have my three levels and I'll put them one behind the other.

Notes

Summary

16m 00s

Gain total



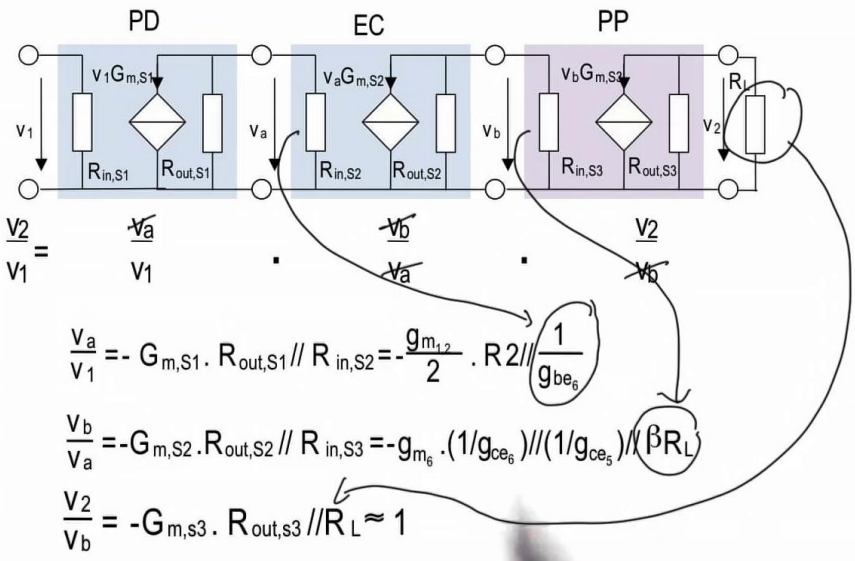
The differential loss, the common-transmitter, and the push-pull. There is the first, independent of the others, it's here. The second too, and the third too. But you know that when you put levels like this, you're forced to calculate the function of the overall gain. It is V2 divided by V1. This is the output of all, this is the entrance of all. And so if I have to take V2 / V1, I have to do: Va / V1 x Vb / Va x V2 / Vb. Each has a transfer function, Look, we simplify this and this, this and this, which gives us V2 / V1 found here. So the three levels, sums up, to take each gain and multiply it by the other. But be careful, if I hide this part, I do Va / V1, now when I plug this level behind look at this resistance: the input resistance of my common-transmitter comes in parallel with the output resistance of my differential pair. So the paralleling of these two, will have an effect on the gain of this. So without this level, you see a gain Gm X this resistance, Now we see a gain Gm X this resistance, parallel with this. This is very important. So we can break everything while plugging incorrectly, so degrading the characteristics, this is not important because we counted on the gain which would be done in the common transmitter, so it's in doing this that we can break the gain.

Notes

Summary

16m 16s

Gain total



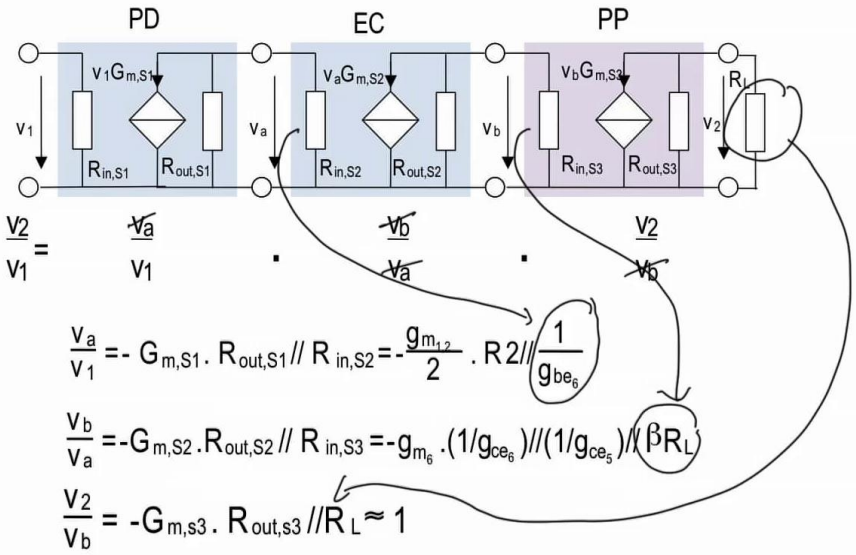
You remember that I wanted to do the gain thanks to these two levels, and I want to say, that the gain is basically done by this level here So we should not degrade the gain, because of a relatively low input impedance. Here I take my expressions and I take into account what has just been added. So this is due to that. So it came in parallel compared to what I'll note before connecting it. Same here. This resistance came in parallel here, So the beta X RL comes here. And here, the resistance RL, is that which the user will connect in open loop, and it comes here. So when I write this, it is precisely to take into account of the input and output impedances, and which come into parallel when I put them one behind the other, and here I am trying to describe my gains Va / V1, Vb / Va, V2 / Vb and I just have to multiply this X this X this, and find the total gain of this setup. So this, will be an exercise I'll give you immediately after this video, you can continue to solve it, there are numerical values and you will see you can achieve fairly high gains with this kind of setup, and make a setup that gives an operational amplifier, realized by three floors.

Notes

Summary

18m 00s

Gain total



Pay close attention to the fact that something is missing in this explanation. You will see it in other lessons, it is to make it stable, that is to say when we do a counter-reaction, it is necessary that we respect</ i> the delay created by the setup, for us to continue having sufficient phase margin for the setup to be stable, is that we have to compensate for this setup by adding the junction capacitance, a Miller capacitance or other compensation techniques, to adjust it, what I have not done in this exercise, so it remains an oriented exercise. Function, analog structure and gain calculations to be implemented, it will be necessary to add the stability study of this type of installation. I'd like to finish this part, I think I just tackled the essential of what we should know about the transistor, the last example we just saw shows us the power of the methods we studied, a more complete exercise that could be very, very useful for someone who would really want to use all the structures we learned to calculate, and all the methodologies that were added, perhaps take a more detailed operational amplifier, or a more complex audio amplifier and achieving it would be a great exercise to do in the continuation of this course.

Notes

Summary

19m 30s