

Les amplificateurs de classe B & AB



- PRINCIPE DE LA CLASSE B
- PRINCIPE DE LA CLASSE AB
- PUISSANCE ET RENDEMENT
- REALISATION PRATIQUE - MONTAGE DE BASE

Electronique II

Good morning everyone. We'll cover in this video the principle of class B followed by a modification of this class B which will become AB that is to say, we will add a little bit of polarization to the transistor to paste a little bit of current passing in our components. We will call it AB. And we will do performance analysis of a type B or AB setup So I will continue to say either B or AB because there is very little current that will pass and that makes the difference and I end with a practical example of an implementation of a single class B amplifier.

Notes

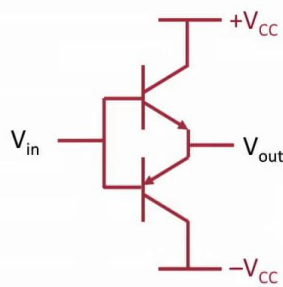
Summary



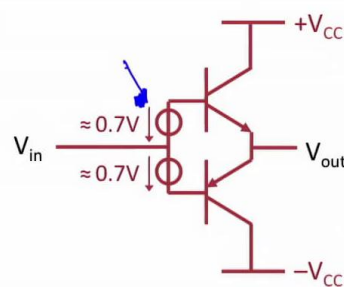
0m 04s

Les amplificateurs de classe B & AB

- Etages de puissance à basse impédance de sortie de type "Push-Pull" à Collecteur Commun ou Drain Commun.
- Chaque transistor prend en charge une demi-alternance du signal.



Classe B



Classe AB

Electronique II

To start the analysis of amplifiers, we'll just see what that means class B. Then we will then talk about class AB. So a class B amplifier, as we had already said in the previous video, This is an amp that will take voltage here convert it into the same voltage it is a voltage follower so it will be a common collector achieved by a push-pull setup to have a symmetrical supply and so that the voltage V_{out} can display a low impedance. So the impedance I see from here, This is the impedance I see from a transmitter of a bipolar transistor It means that it is a low impedance as compared to the one I see from here which is of high impedance compared to this one. We call this class B and this class AB. The only difference between the two, is these voltage sources that I added here. So these pressure points that you see here, are voltage sources which are supposed to polarize the bipolar transistor junction either one or the other, by two voltage sources for the two tensions that we see at the entrance and exit are quite similar in DC and AC.

Notes

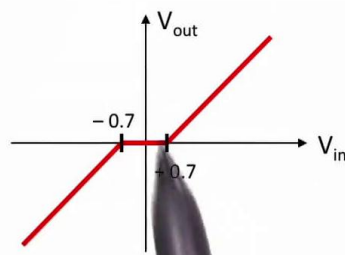
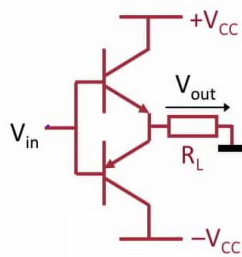
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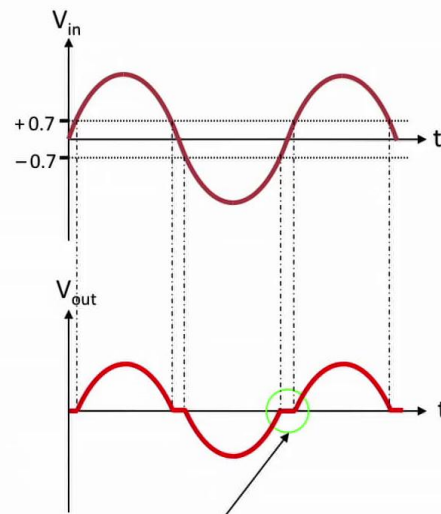
0m 43s

Les amplificateurs de classe B & AB

Les transistors sont polarisés à $V_{BE} = 0$, donc bloqués



Le seuil de ± 0.7 V provoque une distorsion de croisement (cross-over)



Electronique II

This is an example of the class B amplifier that we will immediately turn into AB and see why we need this change to get this A. So the type of amplifier B corresponds to this feature. So if I hide this part, if I just look at the NPN transistor which is above and I look at the charge connected here by putting the right hand over, you'll see that this is indeed a common-collector type of transistor. The collector is connected to a V_{cc} , the load is connected to ground and I have an input voltage. Now if I hide the other transistor, it is again a common collector with the load connected to 0 and the transistor collector is connected to $-V_{cc}$ and I have the input voltage. So I have two transistors that realize the famous Push-Pull setup. So the characteristic of an NPN common header, This is what I see here. So I see that V_{out} and V_{in} are linearly proportional as soon as the transistor begins to conduct, that is to say beyond a junction voltage.

Notes

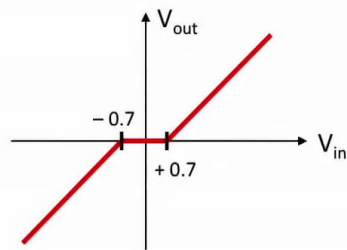
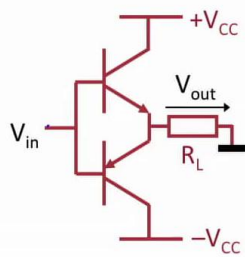
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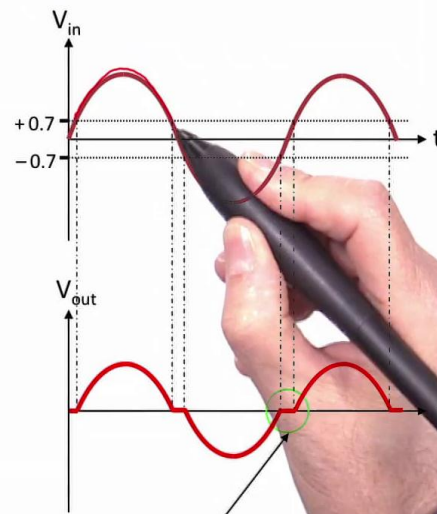
1m 54s

Les amplificateurs de classe B & AB

Les transistors sont polarisés à $V_{BE} = 0$, donc bloqués



Le seuil de ± 0.7 V provoque une distorsion de croisement (cross-over)



I look at the voltage at the output when the input is negative. I see that I have a negative voltage. Of course, it's the same story for the PNP transistor: When the transistor starts conducting, I'm going to have a linear law. So we see that the linearity is from here to there, from here to there. But the two transistors are blocked between more or less a junction voltage for both. So when we talk about this junction voltage which is about 0.7 volts... So we have 0.7 volts, both transistors are blocked and this will create a crossover distortion called cross-over. So when looking at the input voltage and looking at the output, there is still a distortion clearly identified here. When the input voltage exceeds the voltage of junction that's where our transistor will conduct. So we will have a transistor that is conductive right here, just this part here. And here, between this part here, so that what we see in both voltages is roughly 0.7, we'll have the output voltage that will be blocked where both transistors are blocked.

Notes

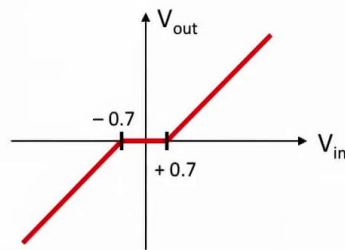
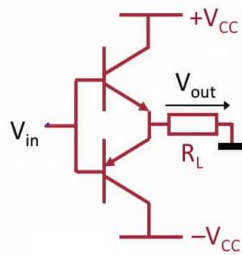
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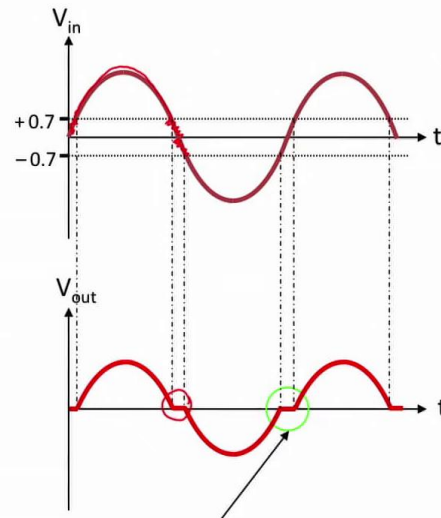
3m 00s

Les amplificateurs de classe B & AB

Les transistors sont polarisés à $V_{BE} = 0$, donc bloqués



Le seuil de ± 0.7 V provoque une distorsion de croisement (cross-over)



Electronique II

So we will find to output a voltage equal to 0. So this distortion here is necessarily audible if it is an audio amplifier. Or if there is another amplifier, we will talk about a distortion. This is a distortion due to the non-polarization of our components. So this is what drives us to do class A. I remind you that the class A, it means that your transistor was polarized throughout the passing period of your input voltage. So we impose only one component to conduct all along the signal. Which leads us to move this voltage, to make it either completely positive or completely negative and to conduct the transistor after having polarized the transistor in the in and out area which we will not do here. There is no test consumption here when there is nothing going on here. We have no input voltage, it would be 0 volts at the exit, so no current is flowing here and no current is flowing through the two transistors. What we are going to change, is to do a little polarization.

Notes

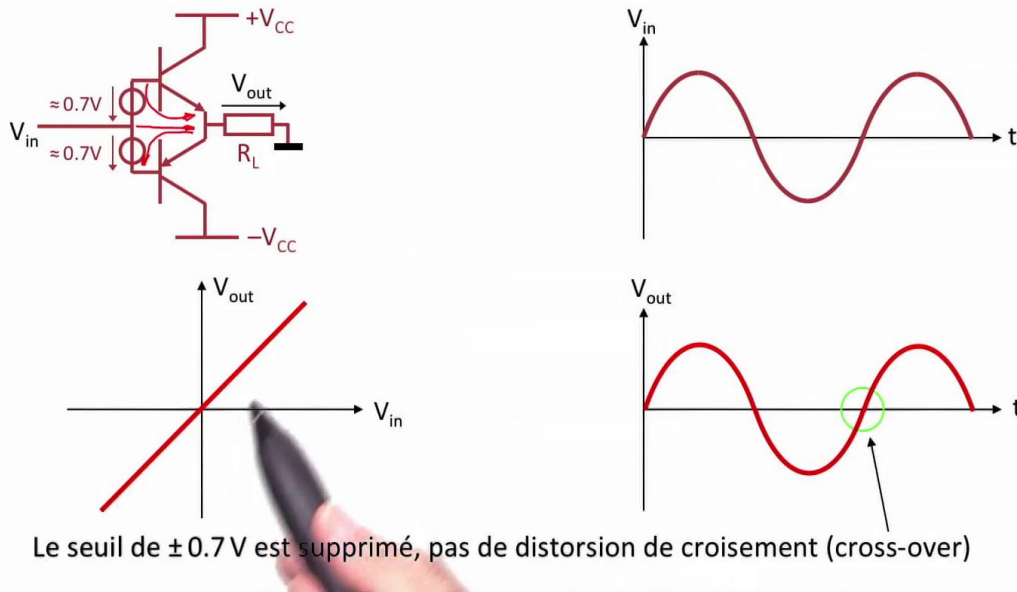
Summary



4m 09s

Les amplificateurs de classe AB

Les transistors sont polarisés ($V_{BE} \approx U_j$) avec un petit courant de repos.



Electronique II

And we'll call this class AB. So I'm going to impose a bit of polarization that is to say there will be a ground that will go to rest without a signal which will pass through the two transistors. What is sent from the NPN transistor will be absorbed by the PNP transistor. So if you look at this diagram here, you will see that I had to add a polarization. I drew it as a voltage. So if you take the 0.7 volt that I added here and you consider that this transistor here, it will conduct because we imposed to it 0.7 and on this side, I have 0.7 volts, you will understand that the potential difference from here to here is 0 DC. So if you put 0 volts here you will find 0 volts here. This will result in an alignment of two characteristics. This way, even if the voltage source here $V = 0$, I am around the origin, I'll find that $V_{out} = 0$ but as soon as the voltage V_n increases, V_{out} will follow.

Notes

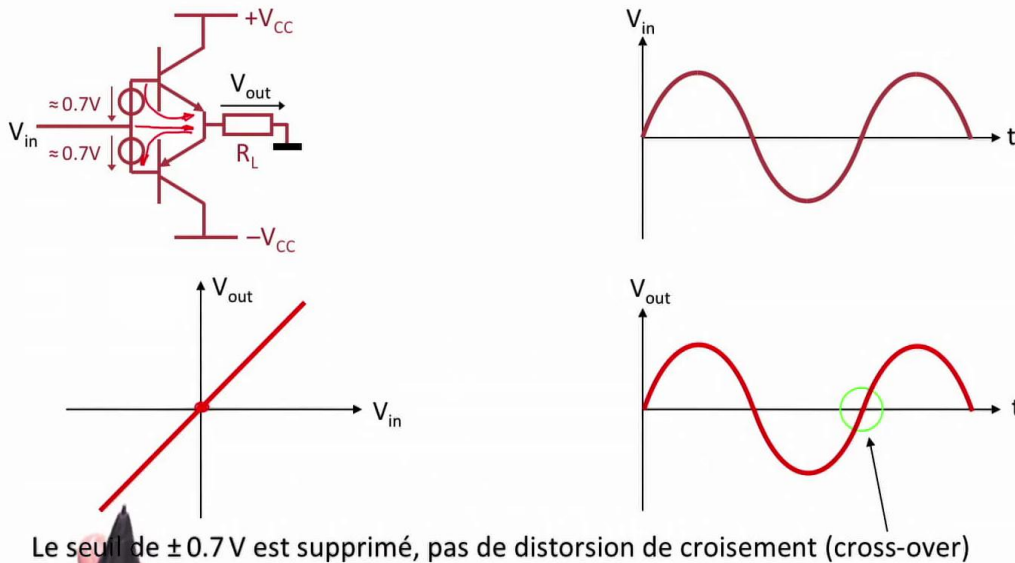
Summary



5m 18s

Les amplificateurs de classe AB

Les transistors sont polarisés ($V_{BE} \approx U_j$) avec un petit courant de repos.



Electronique II

So I have at rest a voltage difference equal to 0 and when I start applying a voltage that increases or decreases, I was able to eliminate this discrepancy between the two voltages. So I deleted this crossover distortion and the input and output is the true copy. So what you put here you find it exactly here in terms of voltage. So it is typical to a voltage follower. The input voltage equals the output voltage, and the current is the current that will pass through the supply controlled by the voltage variation either on this junction when we have a positive voltage, or this junction when we have a negative voltage. So we will have one of the transistors conducting and at rest, we will have very less current. And that's how much we put in class A, that is to say how much we polarized the junction for there to be current flowing here.

Notes

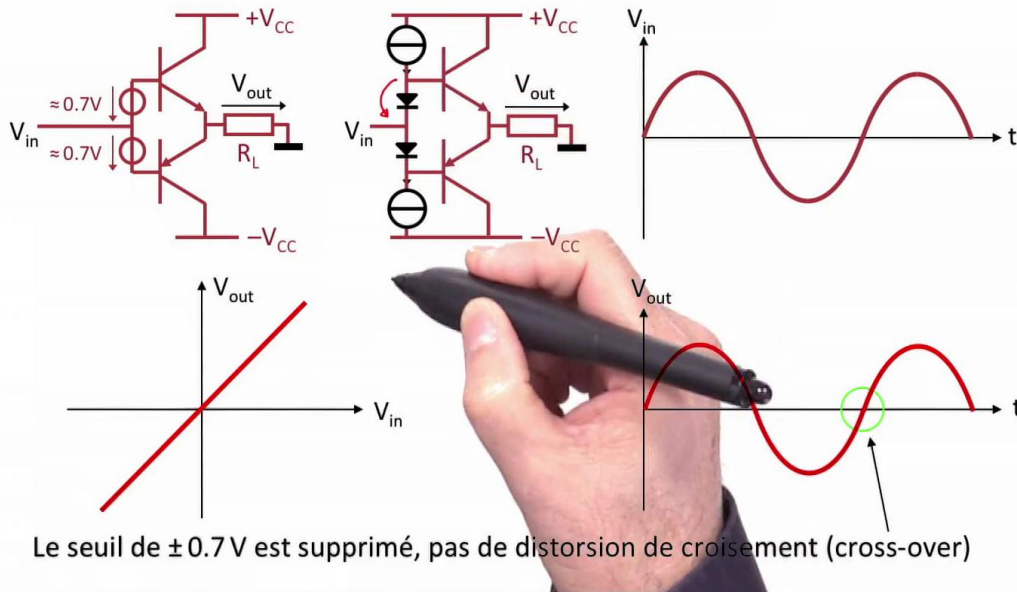
Summary



6m 24s

Les amplificateurs de classe AB

Les transistors sont polarisés ($V_{BE} \approx U_j$) avec un petit courant de repos.



Electronique II

So theoretically, if the two transistors are the same and we impose a voltage that conducts both exactly so that the voltage generated by one is absorbed by the other, we will have 0 current in the charge which is in practice extremely difficult to do because we have two complementary transistors that are not of the same nature, the other an NPN PNP. So in practice, we will have a lot of trouble to avoid that there be a little current going through the charge. But the more we add polarization current in both transistors the better the compensation around this passage by 0 of our feature. To do this, One technique is to use this kind of setup. In this kind of setup, we see that we used the diode to generate the voltage of U_{be} . So I take a junction voltage I impose myself through a diode. I need to create a path for the current. It is necessary that the current flows in that direction. So I will have to connect a positive potential.

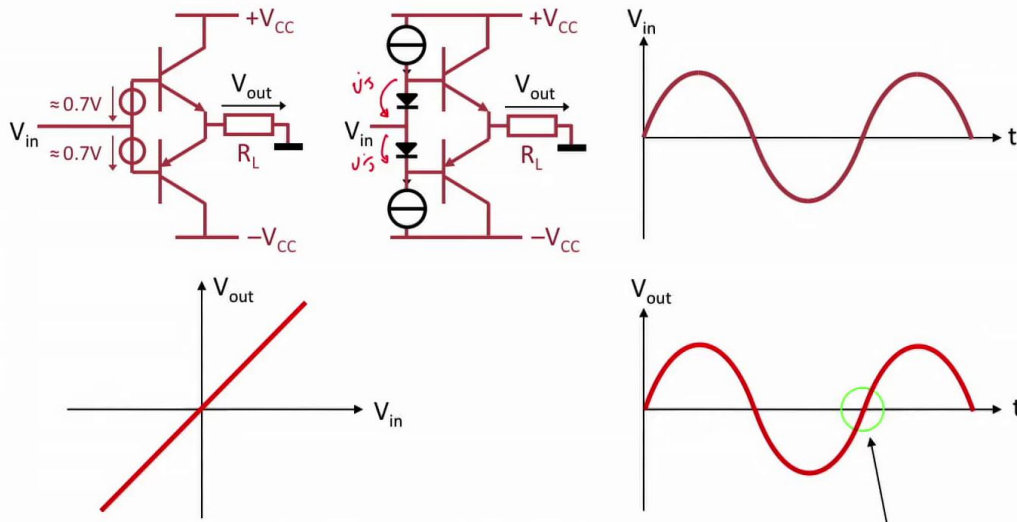
Notes

Summary



Les amplificateurs de classe AB

Les transistors sont polarisés ($V_{BE} \approx U_j$) avec un petit courant de repos.



Le seuil de $\pm 0.7\text{ V}$ est supprimé, pas de distorsion de croisement (cross-over)

Electronique II

Here, I showed that I made it by current sources. This is a theoretical way to show that I have an almost zero voltage from here to here I have an almost zero voltage from here to here because there is a supply source it is current even if the difference in voltage is equal to 0 and you will be able to impose a current which passes through the two diodes and this current then depends on the current you have put which will generate junction voltage across a diode and the same across a diode that are expected to generate two junction voltages. It's that we fall back at this moment in this situation and we get a practical implementation for the creation of polarization of the output level. And there, we can find what we saw earlier that is to say an input voltage equals the output voltage and a gain is 1 in this kind of setup with a current gain which is extremely high which is proportional to β gain of the bipolar transistors we used. That is to say, the current entering here corresponds to β times the current that goes out of the other side.

Notes

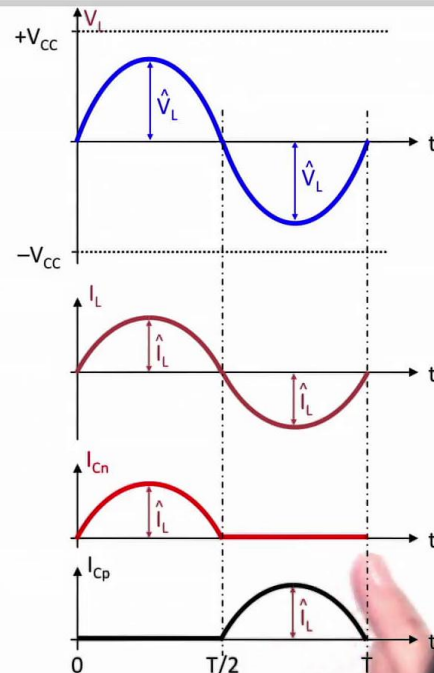
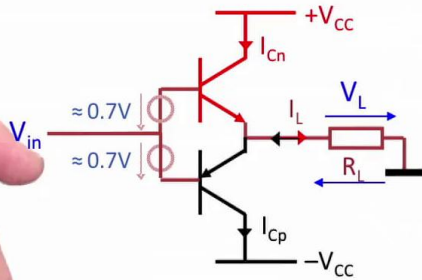
Summary



8m 22s

Principe des amplis classe B

Chaque transistor prend en charge une demi-alternance du signal, l'un la positive, l'autre la négative.



Electronique II

I'll analyze this setup in more details to understand what will happen in terms of power. So each transistor supports a half-alternation signal. One, the positive alternation, the other, a negative alternation. So if you take the input V_{in} and you this voltage here. We imagine it is a voltage of this style. What will happen? You'll have your transistor in red that will begin to conduct current that I've drawn in red. So there will be a collector current of the NPN transistor that will always be in red in the charge. So the voltage V_L , if this voltage increases, this current will pass into the charge. This voltage will follow it in the same amount. I drew this in this way. I have shown that for the positive alternation so when you we're here, I'm going to draw, shade this in red, I see that there is a current that will pass through the transistor N and will go to the charge and then, I'll get to block this transistor when I lower this voltage.

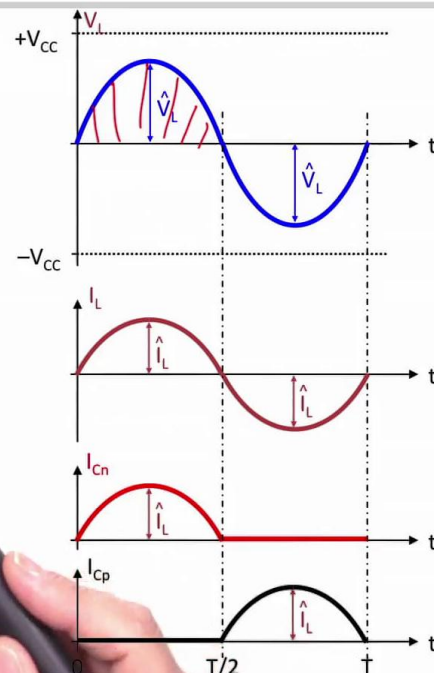
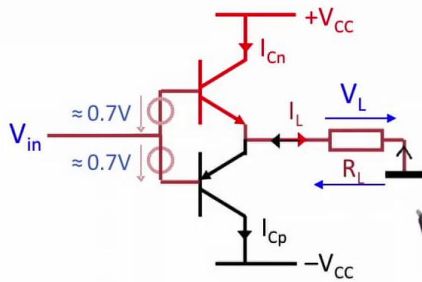
Notes

Summary



Principe des amplis classe B

Chaque transistor prend en charge une demi-alternance du signal, l'un la positive, l'autre la négative.



Electronique II

Because when I lower the voltage, this transistor here blocks. I have a junction here that will have a voltage and this voltage then begins to follow rather this one that begins to be negative. So when I lower this voltage, the transistor here will start to conduct and it is the black arrow So I'm having a black current that will pass through the charge like this and will continue its path and it will generate a voltage will be positive in this direction in the charge. So current flows through the PNP transistor, This is the current that is here. The sum of the two currents, is the two currents that will appear in the charge. So if I take... sorry, I'm talking of the sum If I speak of the sum while considering the arrow I now speak in terms of voltage The voltage will reflect the current $I \times R$ When the current is positive in this direction. So I will see that V_L will be positive in that sense. Otherwise, as I power to $-V_{cc}$, I will have a current flowing in that direction and V_L that will be negative in this direction.

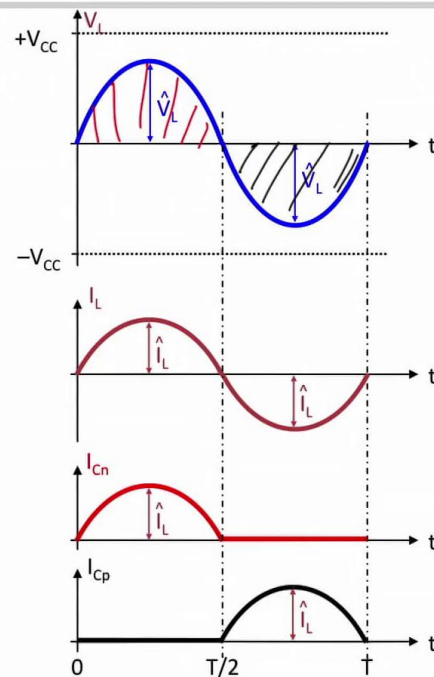
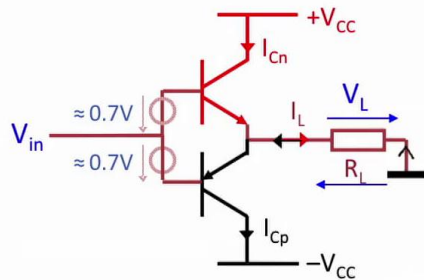
Notes

Summary



Principe des amplis classe B

Chaque transistor prend en charge une demi-alternance du signal, l'un la positive, l'autre la négative.



Electronique II

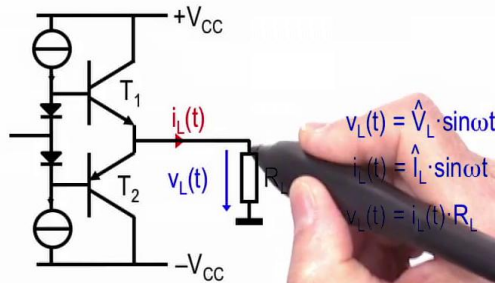
So I will have V_L that will be positive and negative which is exactly the image of what I see about this feature here. So I have a positive voltage. I have a voltage that will be proportional to what I called the black part that is to say, the PNP transistor which is in the process of conducting current that goes in this direction, towards $-V_{cc}$.

Notes

Summary



PUISSANCE (MOYENNE) DANS LA CHARGE R_L EN REGIME SINUS



Pour le calcul théorique des puissances, on admet que :

$$V_{L,crête,max} = V_{CC}$$

Puissance moyenne dans la charge pour un signal sinus :

$$P_{RL} = \frac{V_{L,eff}^2}{R_L} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

$$P_{RL,max} = \frac{V_{CC}^2}{2 \cdot R_L} \quad \text{Maximum théorique}$$

Electronique II

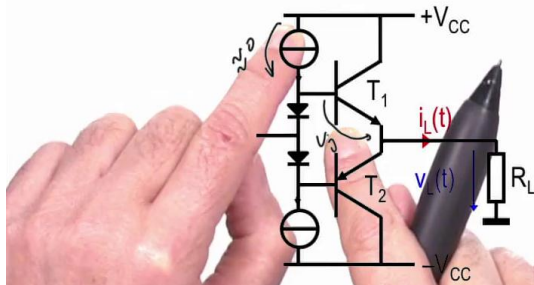
Coming from the performance performance. So the performance of such a setup and we will take again what we mentioned at the beginning we will look at the average power expressing the instantaneous power and we will look at both the expression of the instantaneous power then, calculate the average power. So I start with a medium voltage with a voltage... pardon, the value of the average power with a sinusoidal voltage. I applied to the input a voltage $V(t)$ that will be the same $V_L(t)$ since it is the true copy of both. And we will find that $V_L(t) = \hat{V}_L \sin \omega t$ will of course generate a current that will be $\hat{I}_L \sin \omega t$ and Ohm's law is what will connect these two expressions together. to simplify the calculation that will follow. When I look at a transistor like this, then I want to see which is the maximum voltage that appears there. Remember that this voltage, I look on the transmitter.

Notes

Summary



PUISSANCE (MOYENNE) DANS LA CHARGE R_L EN REGIME SINUS



$$\begin{aligned} v_L(t) &= \hat{V}_L \cdot \sin \omega t \\ i_L(t) &= \hat{I}_L \cdot \sin \omega t \\ v_L(t) &= i_L(t) \cdot R_L \end{aligned}$$

Pour le calcul théorique des puissances, on admet que :

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$$P_{RL, \text{max}} = \frac{V_{CC}^2}{2 \cdot R_L} \quad \text{Maximum théorique}$$

Electronique II

<I> When I look at a voltage on the transmitter and </ i> <I> I consider myself that I have a voltage here </ i> <I> which is a junction voltage </ i> <I> and that this voltage source </ i> <I> or the voltage difference here can be 0, </ i> <I> if it is a current source </ i> <I> therefore I can fully impose a voltage equal to 0. </ I> <I> In practice, there would be here a transistor instead of this </ i> <I> but whose collector is connected here. </ I> <I> That means that I can push this voltage </ i> <I> up to about 200 millivolts </ i> <I> before $U_{ce} = 200$ millivolts </ i> <I> even if it is said that $U_{ce} = 0$ the transistor is saturated, </ i> <I> in practice one needs low power transistors </ i> <I> in the order of magnitude of 200 millivolts </ i> <I> so that the transistor does not go into direct saturation. </ I> <I> So if I push this voltage here, </ i> <I> the junction voltage remains the same. </ I> <I> So this one will follow </ i> <I> until I get to saturate this transistor here. </ I> <I> So if this voltage equals 0, </ i> <I> that means, to allow for the maximum voltage </ i> <I> I see here, I have to go through</ i> <I> the feature like this.

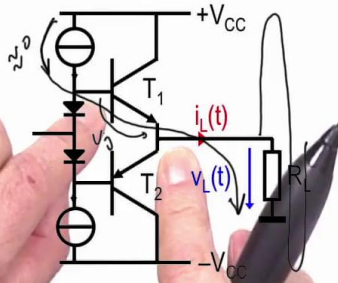
Notes

Summary



13m 11s

PUISSANCE (MOYENNE) DANS LA CHARGE R_L EN REGIME SINUS



$$\begin{aligned} v_L(t) &= \hat{V}_L \cdot \sin \omega t \\ i_L(t) &= \hat{I}_L \cdot \sin \omega t \\ v_L(t) &= i_L(t) \cdot R_L \end{aligned}$$

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Electronique II

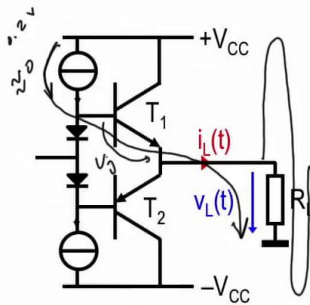
That's the way I would have looked to say what is the voltage $V_{out \text{ max}}$. Why am I talking about this? Because I'm going to simplify in the calculation that follows. This voltage, will rise up to what value? It could rise to $V_{CC} +$ and go down to $-V_{CC}$. In practice, no. Does it depends on the saturation of this transistor? Absolutely not. It depends on the junction here. Look at the way I have to go when I look from the transmitter. From the transmitter of a transistor, I have my two fingers which will rise in the same amount until I saturate this current source. And I stop at a difference when this voltage here is equal to this. So I have a short circuit from here to there, I have 0 volts. In theory, it will still have this voltage and this the equivalent of a voltage U_g . This voltage max, it will be at $V_{CC} - U_g$. In practice, we must add the equivalent of something like 0.2 volts when bringing a transistor where the transmitter is connected here and the collector is connected here.

Notes

Summary



PUISSANCE (MOYENNE) DANS LA CHARGE R_L EN REGIME SINUS



$$\begin{aligned} v_L(t) &= \hat{V}_L \cdot \sin \omega t \\ i_L(t) &= \hat{I}_L \cdot \sin \omega t \\ v_L(t) &= i_L(t) \cdot R_L \end{aligned}$$

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Electronique II

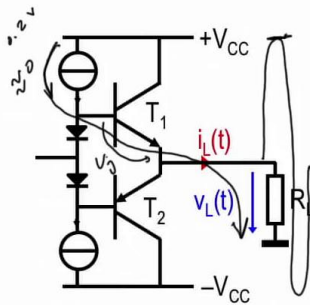
Or we must consider the voltage difference we have seen on this power source once achieved with transistors. So in practice, the maximum voltage is proportional to V_{CC} minus the necessary voltage for this current source to remain the current source to which must also subtract the voltage U_g . But in the calculation that follows, I will take this into account: I will consider the voltage, it can rise to V_{CC} . In other words, I am saying I neglect this voltage drop U_g I'm talking and I neglect this small voltage drop that I need to reserve for my source. So I will consider in my calculation this hypothesis that is written here so not to say all the time and this V_{CC} minus the saturation voltage here minus the voltage U_g of this transistor, I will approximate this all the time to V_{CC} . So by writing the law in the power or power in charge, it is a power which is equal to the efficient value divided by the value of the charge.

Notes

Summary



PUISSANCE (MOYENNE) DANS LA CHARGE R_L EN REGIME SINUS



$$\begin{aligned} v_L(t) &= \hat{V}_L \cdot \sin \omega t \\ i_L(t) &= \hat{I}_L \cdot \sin \omega t \\ v_L(t) &= i_L(t) \cdot R_L \end{aligned}$$

Pour le calcul théorique des puissances, on admet que :

$$V_{L, \text{crête, max}} = V_{CC}$$

$$= -(V_{s, \text{sat}} + V_{CE}) + V_{CC}$$

Puissance moyenne dans la charge pour un signal sinus :

$$P_{RL} = \frac{V_{L, \text{eff}}^2}{R_L} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

$$P_{RL, \text{max}} = \frac{V_{CC}^2}{2 \cdot R_L} \quad \text{Maximum théorique}$$

Electronique II

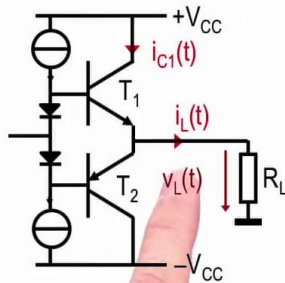
I always replaces the efficient value by the peak value because this is what interests me before saturating. So I want to talk about this saturation voltage. And then in this case, I say I can go up until V_{CC} up. So the maximum power in the charge is slightly above this. And theoretically, according to this hypothesis here it is equal to V_{CC} divided by $2 \cdot R_L$. So for a quick calculation, I can accept this if not, I have to calculate where I say V_L peak = U we'll call this voltage source and I'll talk about saturation. So what is the saturation voltage to allow for this setup less... Excuse all this plus U_{CE} and I have to put a - sign and subtract this from V_{CC} . So here I wrote it wrongly. I will note more clearer the voltage U_{CE} . So V_{CC} minus V_{CE} minus the saturation voltage here plus the U_{CE} I will subtract to talk in practice about this true peak voltage. And we will approximate it by V_{CC} .

Notes

Summary



PUISSANCE INSTANTANÉE DISSIPÉE DANS LES TRANSISTORS



Puissance instantanée dans T_1 :
(par symétrie, le résultat est identique pour T_2)

$$p_{Q1}(t) = v_{CE1}(t) \cdot i_{C1}(t)$$

$$p_{Q1}(t) = (V_{CC} - v_L(t)) \cdot i_L(t) = (V_{CC} - v_L(t)) \cdot \frac{v_L(t)}{R_L}$$

$$= V_{CC} \frac{v_L(t)}{R_L} - \frac{v_L^2(t)}{R_L}$$

La puissance instantanée est maximum pour :

$$\frac{\delta p_{Q1}(t)}{\delta v_L(t)} = \frac{V_{CC} - 2v_L(t)}{R_L} = 0$$

$$\Rightarrow v_L(t) = \frac{V_{CC}}{2} \quad \text{et} \quad p_{Q1,max} = \frac{V_{CC}^2}{4 \cdot R_L}$$

La valeur de la puissance instantanée est importante pour les signaux $v_L(t)$ de très basse fréquence, vu la faible inertie thermique des jonctions des transistors

Electronique II

I will now take the same set up, realize it as it was and go into the expression of the power that will take me to express the efficiency of such a setup. The power... I will start by analyzing the power that is dissipated in the load. I just saw the one that was in my charge, sorry. This is the expression that I have seen just now and now I will express the one I see in my transistor. Take the example of NPN transistors I can do the same for the PNP. This transistor here has a voltage difference multiplied by a current here. So that, it will give me the instant expression of power I'll dissect as $V_{CC} - V_n$ this is the V_{ce} voltage. So this voltage, is all the time... The V_{ce} is less tension this voltage I see across the load, So it will give me this term multiplied by the current flowing through the transistor, which is exactly the current charge. So this current $I_{c1} = I_L$. I know the expression.

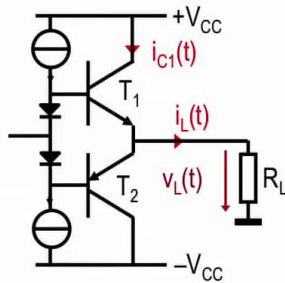
Notes

Summary



17m 46s

PUISSANCE INSTANTANÉE DISSIPÉE DANS LES TRANSISTORS



Puissance instantanée dans T_1 :
(par symétrie, le résultat est identique pour T_2)

$$p_{Q1}(t) = v_{CE1}(t) \cdot i_{C1}(t)$$

$$p_{Q1}(t) = (V_{CC} - v_L(t)) \cdot i_L(t) = (V_{CC} - v_L(t)) \cdot \frac{v_L(t)}{R_L}$$

$$= V_{CC} \frac{v_L(t)}{R_L} - \frac{v_L^2(t)}{R_L}$$

La puissance instantanée est maximum pour :

$$\frac{\delta p_{Q1}(t)}{\delta v(t)} = \frac{V_{CC} - 2v_L(t)}{R_L} = 0$$

$$\Rightarrow v_L(t) = \frac{V_{CC}}{2} \quad \text{et} \quad p_{Q1,max} = \frac{V_{CC}^2}{4 \cdot R_L}$$

La valeur de la puissance instantanée est importante pour les signaux $v_L(t)$ de très basse fréquence, vu la faible inertie thermique des jonctions des transistors

Electronique II

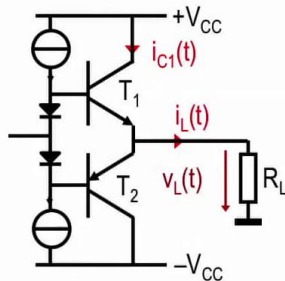
It is Ohm's law that will give it to me: it is the voltage across my terminals divided by the resistance of the charge. So I replace it with its value. I performs the multiplication and I found the instantaneous power dissipated in my transistor is equal to V_{CC} when V_L divided by R_L least square value V_L divided by R_L . So I have a square law function of the output voltage which is the V_L which is X^2 over R with a -sign an X / R multiplied by a constant which is the voltage V_{CC} . If you consider what happens in an a setup containing a signal that varies very little over time so something that is very very very small in variation, the instant power, it could be important when there is a certain inertia of low frequency because we have the junction of the transistor that will eventually heat and that thermal heating could be of interest us when we speak of a very low frequency signal. That's why I'll search for when does the instantaneous power reaches a maximum.

Notes

Summary



PUISSANCE INSTANTANÉE DISSIPÉE DANS LES TRANSISTORS



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(par symétrie, le résultat est identique pour T_2)

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La valeur de la puissance instantanée est importante pour les signaux $v_L(t)$ de très basse fréquence, vu la faible inertie thermique des jonctions des transistors

Electronique II

So looking at this, I see that the expression I have here by deriving it in the function of voltage I see $V(t)$ which is over the charge or on entry and that I equate to 0 to see the maximum I see it is when the voltage on my charge is equal to half the supply voltage at that time, I have maximum power dissipated in one or the other transistor So this power, is worth $V_{CC}^2 / 4 \times R_L$. That is the maximum instantaneous power in a transistor when the signal is at low frequency. I will now move to the average power. So I'll take this phrase that I have here.

Notes

Summary



PUISSANCE (MOYENNE) DISSIPÉE DANS LES TRANSISTORS EN RÉGIME SINUSOÏDALE

La puissance moyenne durant une période P_Q , est égale à la puissance moyenne dissipée dans chacun des 2 transistors durant la demi-période où il est actif.

$$P_Q = \frac{2}{T} \cdot \int_0^{T/2} v_{CE}(t) \cdot i_C(t) \cdot dt = \frac{2}{T} \cdot \int_0^{T/2} [V_{CC} - v_L(t)] \cdot \frac{v_L(t)}{R_L} \cdot dt$$

$$= \frac{1}{\pi} \cdot \int_0^{\pi} [V_{CC} - \hat{V}_L \sin \alpha] \cdot \frac{\hat{V}_L \sin \alpha}{R_L} \cdot d\alpha = \frac{2 \cdot V_{CC} \cdot \hat{V}_L}{\pi \cdot R_L} - \frac{\hat{V}_L^2}{2 \cdot R_L}$$

P_Q est maximum pour :

$$\frac{\delta P_Q}{\delta \hat{V}_L} = \frac{2 \cdot V_{CC}}{\pi \cdot R_L} - \frac{\hat{V}_L}{R_L} = 0 \Rightarrow \hat{V}_L = \frac{2 \cdot V_{CC}}{\pi} \text{ et } P_{Q,max} = \frac{2 \cdot V_{CC}^2}{\pi^2 \cdot R_L} \approx 0.2 \cdot \frac{V_{CC}^2}{R_L}$$

Electronique II

I will apply a sinusoidal voltage to this kind of setup and I'll look at the average power. This is the one we look at quite often to watch what the average loss value in the transistor. We have already discussed this kind of expression when introducing in the previous video. So how will I address this? I have two transistors. I know that each of the transistor will conduct during half the period. So I just have to take the average power in a transistor and multiply by a factor of 2 what I'm doing here. So the average power in a transistor is the voltage times the current route. I include over half of the period because this transistor is blocked. So it just goes... What concerns me is when it sees the current pass multiplied by $1/T$ and I multiply by 2 I speak of power in both transistors knowing that each working for half the period. I take the calculated expression just now it's here.

Notes

Summary



PUISSANCE (MOYENNE) DISSIPÉE DANS LES TRANSISTORS EN RÉGIME SINUSOÏDALE

La puissance moyenne durant une période P_Q , est égale à la puissance moyenne dissipée dans chacun des 2 transistors durant la demi-période où il est actif.

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P_Q est maximum pour :

$$\frac{\partial P_Q}{\partial \hat{V}_L} = \frac{2 \cdot V_{CC}}{\pi \cdot R_L} - \frac{\hat{V}_L}{R_L} = 0 \Rightarrow \hat{V}_L = \frac{2 \cdot V_{CC}}{\pi} \text{ et } P_{Q,max} = \frac{2 \cdot V_{CC}^2}{\pi^2 \cdot R_L} \approx 0.2 \cdot \frac{V_{CC}^2}{R_L}$$

Electronique II

I replace the voltage with a sinusoidal voltage. So $\sin \omega t$ by replacing ωt with α . I call a substitution α to write less... it's not all the time ωt and I replace the power that I know on the charge of a sinusoidal voltage that I report here. This is the value of $\hat{v} \sin \omega t$ divided by the value of R that corresponds to the current going through through my office. And I effect the intergral. I replaced with the terminals and I find this phrase. So the average power dissipated in a transistor multiplied by 2 equal to $2 \times V_{CC} \times \hat{v} / \pi \times R_L$ minus \hat{V}^2 / R_L and I look when will that mean power be maximum. So I drift from the variable that is \hat{V}_L . For any value of \hat{V} of the sinusoidal voltage that I apply to such a setup I'm having a maximum average power? Well I'll find that when $\hat{V}_L = 2 V_{CC} / \pi$. It's a calculation to do. It is taken from the derivative of that expression and now I look at the power in the transistor its exact value, replacing \hat{V}_L value not its value which is equal to $2 V_{CC} / \pi$.

Notes

Summary



PUISSANCE (MOYENNE) DISSIPÉE DANS LES TRANSISTORS EN REGIME SINUSOÏDALE

La puissance moyenne durant une période P_Q , est égale à la puissance moyenne dissipée dans chacun des 2 transistors durant la demi-période où il est actif.

$$P_Q = \frac{2}{T} \cdot \int_0^{T/2} v_{CE}(t) \cdot i_C(t) \cdot dt = \frac{2}{T} \cdot \int_0^{T/2} [V_{CC} - v_L(t)] \cdot \frac{v_L(t)}{R_L} \cdot dt$$

$$= \frac{1}{\pi} \cdot \int_0^{\pi} [V_{CC} - \hat{V}_L \sin \alpha] \cdot \frac{\hat{V}_L \sin \alpha}{R_L} \cdot d\alpha = \frac{2 \cdot V_{CC} \cdot \hat{V}_L}{\pi \cdot R_L} - \frac{\hat{V}_L^2}{2 \cdot R_L}$$

P_Q est maximum pour :

$$\frac{\delta P_Q}{\delta \hat{V}_L} = \frac{2 \cdot V_{CC}}{\pi \cdot R_L} - \frac{\hat{V}_L}{R_L} = 0 \Rightarrow \hat{V}_L = \frac{2 \cdot V_{CC}}{\pi} \text{ et } P_{Q,max} = \frac{2 \cdot V_{CC}^2}{\pi^2 \cdot R_L} \approx 0.2 \cdot \frac{V_{CC}^2}{R_L}$$

Electronique II

And this is the average maximum term in a transistor in the case of a sinusoidal excitation. This is $0.2 V_{CC}^2 / R_L$ assuming of course that $\hat{V}_L = 2 V_{CC} / \pi$ and taking into account this term that has been derived from the average value. Remember this. We now see what is the average power to a sinusoidal voltage in a type B or AB setup.

Notes

Summary



PUISSANCE (MOYENNE) DISSIPÉE DANS LES TRANSISTORS EN RÉGIME SINUSOÏDALE

$$P_{\text{alim}} = 2 \cdot V_{CC} \cdot I_{C,\text{moy}} = 2 \cdot V_{CC} \cdot \frac{\hat{V}_L}{\pi \cdot R_L} \quad \text{Rappel : } P_{RL} = \frac{V_{L,\text{eff}}^2}{R_L} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

Ces puissances sont maximum pour $\hat{V}_{L,\text{max}} = V_{CC}$

$$P_{\text{alim,max}} = \frac{2 \cdot V_{CC}^2}{\pi \cdot R_L} \quad P_{RL,\text{max}} = \frac{V_{CC}^2}{2 \cdot R_L}$$

RENDEMENT EN RÉGIME SINUS

$$\eta = \frac{P_{RL}}{P_{\text{alim}}} = \frac{\pi \cdot \hat{V}_L}{4 \cdot V_{CC}} \quad \text{pour } \hat{V}_{L,\text{max}} = V_{CC} : \quad \eta_{\text{max}} = \frac{\pi}{4} = 0.785$$

Electronique II

A short summary to now see the performance. The supply voltage: I remind you that we have a more or less V_{CC} voltage so I have a voltage of $2 V_{CC}$ multiplied by the current that will be carried by the power... which is the current share of this power supply which will be the current that is supplied to the charge. So what is the expression that we know, we just saw. It is $\hat{V}_L / \pi R_L$. Knowing that in the charge we have the $\hat{V}^2 / 2 R_L$ and the supply voltage, So replacing \hat{V}_L by the value we put the hypothesis that is to say $V_{L,\text{max}} = V_{CC}$, the supply should provide a setup class B or AB of the order of magnitude of $2 V_{CC}^2 / \pi R_L$ so that the load times maximum power $V_{CC}^2 / 2 R_L$. So I can calculate my performance. I consider practically, that polarization takes nothing and the little A that I put into it does not count. I divide this by this and I fall back on a value of a maximum performance in the order of 80%. This is equal to $\pi / 4$.

Notes

Summary

24m 00s



PUISSANCE (MOYENNE) DISSIPÉE DANS LES TRANSISTORS EN RÉGIME SINUSOÏDALE

$$P_{\text{alim}} = 2 \cdot V_{CC} \cdot I_{C,\text{moy}} = 2 \cdot V_{CC} \cdot \frac{\hat{V}_L}{\pi \cdot R_L} \quad \text{Rappel : } P_{RL} = \frac{V_{L,\text{eff}}^2}{R_L} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

Ces puissances sont maximum pour $\hat{V}_{L,\text{max}} = V_{CC}$

$$P_{\text{alim,max}} = \frac{2 \cdot V_{CC}^2}{\pi \cdot R_L} \quad P_{RL,\text{max}} = \frac{V_{CC}^2}{2 \cdot R_L}$$

RENDEMENT EN RÉGIME SINUS

$$\eta = \frac{P_{RL}}{P_{\text{alim}}} = \frac{\pi \cdot \hat{V}_L}{4 \cdot V_{CC}} \quad \text{pour } \hat{V}_{L,\text{max}} = V_{CC} : \quad \eta_{\text{max}} = \frac{\pi}{4} = 0.785$$

Electronique II

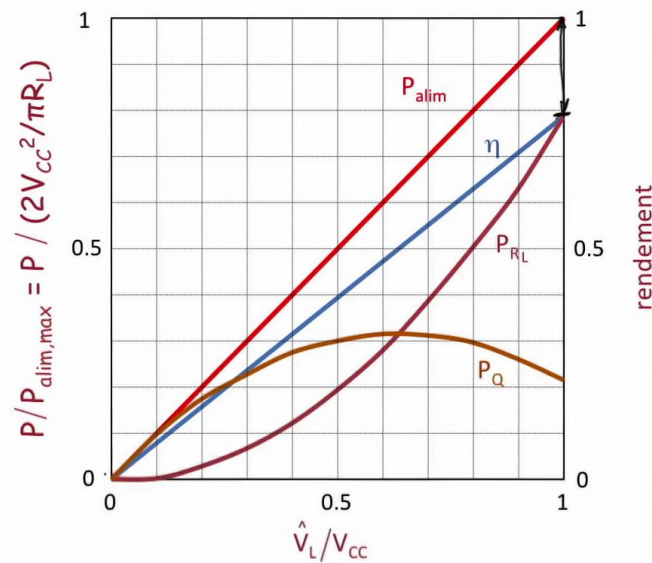
So this is about the 80%. So we can say that the setup of type B or AB has a yield of this order of magnitude, of 78% of what we give it as energy. Compared to a class A, it was found was 25% and there you come across something where you have a loss of 20% and where it falls on a much better yield In a class.

Notes

Summary



Puissances et rendement



Electronique II

This curve summarizes what we just saw. By standardizing the peak value V_{CC} that is to say, when I look $\hat{V}_L = V_{CC}$, there on the scale, I have 1 and normalizing the power I have both in my transistor and in both my office in relation to the supply power, $P_{alim,max}$. So I could say that the maximum power, that's when I have $\hat{V}_L = V_{CC}$ since it is the power supplied by the power which is the normalization value. I saw that the transistor, it has a square law with a \hat{V}_L^2 with a - sign. And in the charge, the \hat{V}_L^2 is divided by R_L . And the performance, I have a loss from here to here that the supply gives and I have all that which is made to the charge. So a visual analysis of this lets us understand everything that is going on inside. How the power transistor takes to a certain value which is of the order of $1/2 V_{CC}$. Then we have the charge that begins to take power and tends towards the maximum power we see here. And it is at that point, we have the maximum yield that's about 20% loss with respect to what the supply gives and compared to what the charge takes as effective value P_Q co power in the charge.

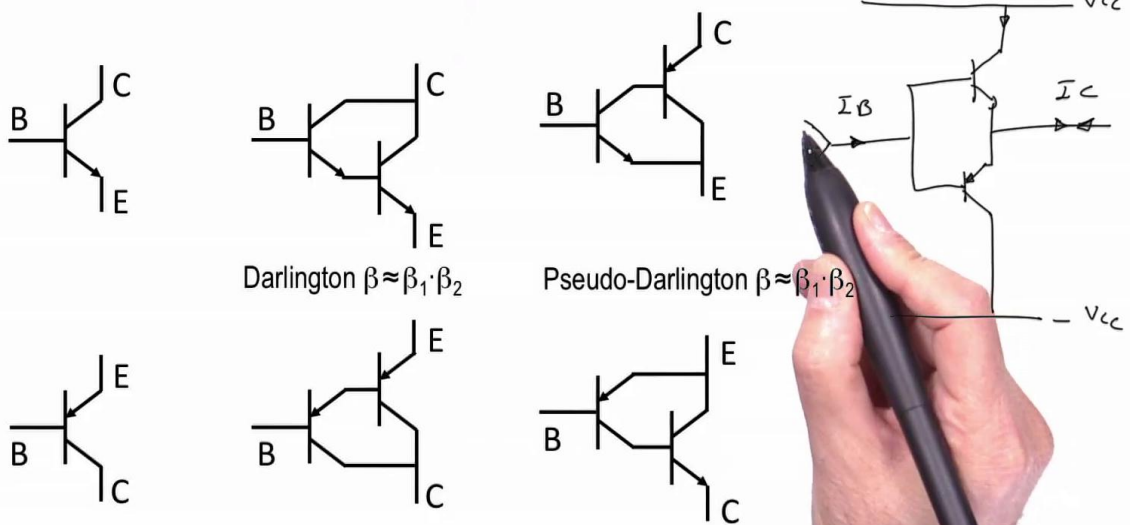
Notes

Summary



25m 51s

Evolution du montage élémentaire



La forte augmentation du β réduit considérablement le courant de base

Electronique II

Let the practical realization. If you remember our Push-Pull setup which was with one NPN-type transistor, 1 PNP transistor type. Both are connected by their emitter. A little polarization here. I'll take the class B and a power supply, an outlet, an inlet and a dual power supply. The current flowing to the outlet is the current that we take from the supply voltage. It is this current that will go in one direction or another. Now, the current that we will take from the level which is just before the one that provides the voltage to our power amplifier class B, it's here. So that's the current I_b and that's the current I_c . What is between the two $I_c = \beta I_b$, such that β is the β of the transistor. Usually, when we do an amplifier level that comes here often, we need to achieve a voltage amplifier there. So here we have a voltage gain and we do a counter reaction between the output and the input with a counter reaction rate that would happen like this.

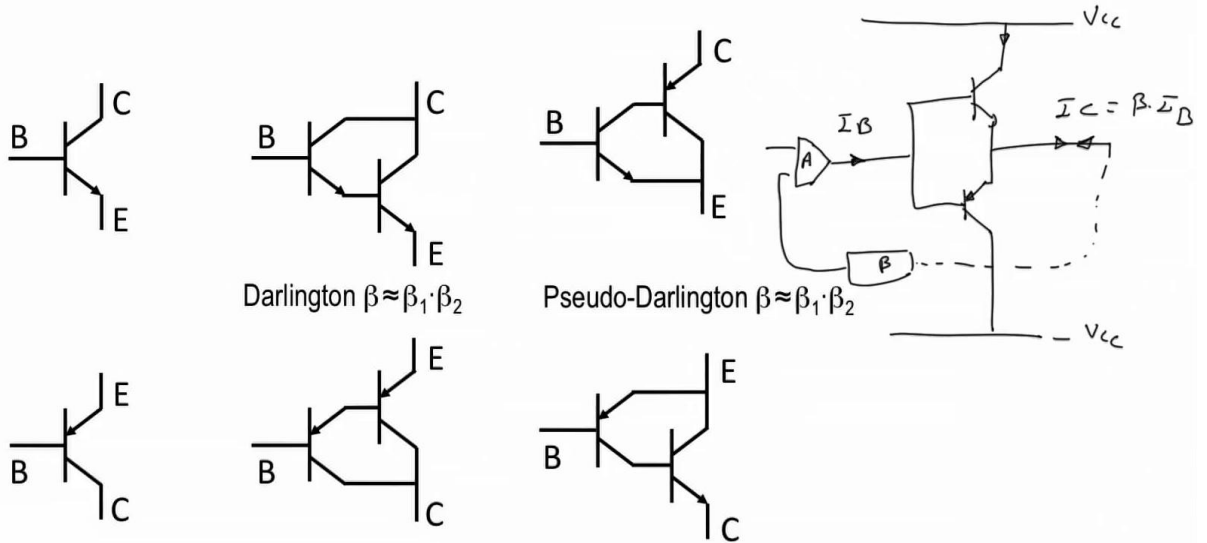
Notes

Summary



27m 28s

Evolution du montage élémentaire



La forte augmentation du β réduit considérablement le courant de base

Electronique II

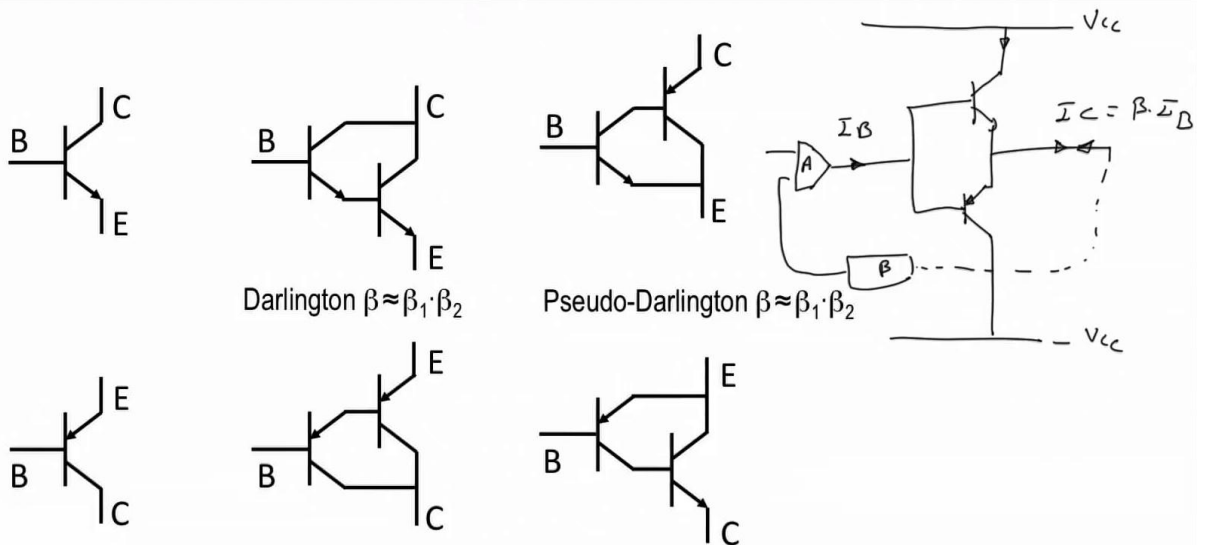
That is the classical setup of a class AB amplifier. The power level is of class AB, plus an amplifier that performs voltage and counter reaction to cause the output voltage subtracted from the input voltage and make all these with a voltage gain proportional to what has been set here. So the most important thing, is what is the relationship between I_b and I_c . It goes through the β because it is $\beta \times I_b$. When a question arises what is the β value in the transistor especially as this is a power transistor, we'll realize that the β of a power transistor is relatively small because the base width of such a transistor can not be very large to have bounds in quite high voltage. When you want to subject this transistor to relatively high voltages, the β can not be very great. We have to have transistors whose β is quite moderate or even low and we require voltage differences at the terminals of this transistor. Which brings us to remedy this β by electronics.

Notes

Summary



Evolution du montage élémentaire



La forte augmentation du β réduit considérablement le courant de base

Electronique II

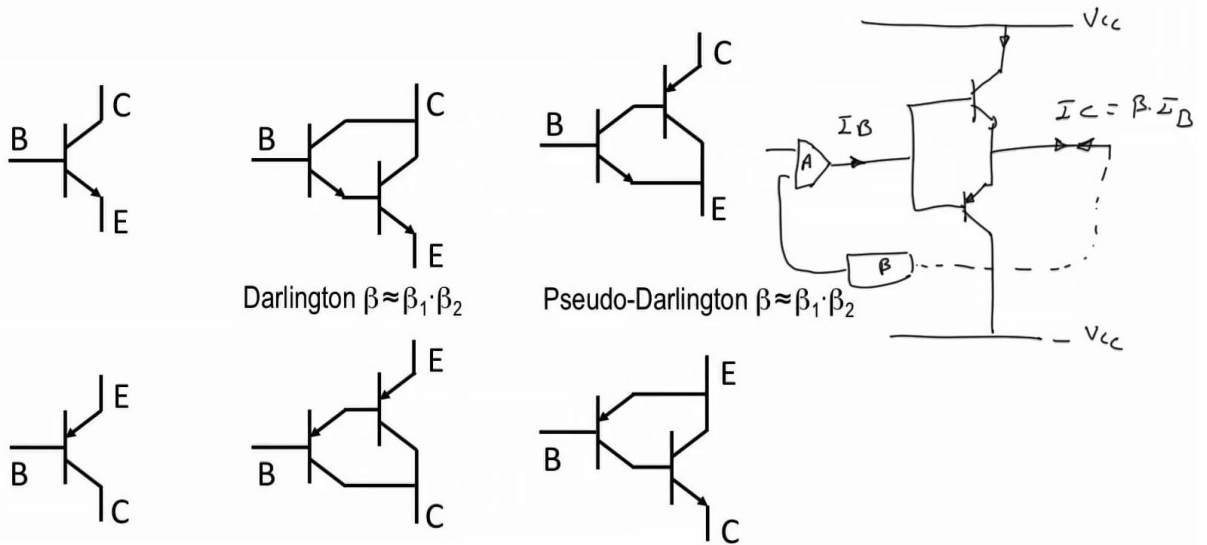
That is to say, we take our component, and replace it by a Darlington. Very often in these amplifiers, if it's realized with bipolar transistors the transistor which performs the setup is often performed by Darlington based fixtures or pseudo-Darlington. So we see here the two possible layouts. When you want to make a Push-Pull, we put this transistor here and replace it by the equivalent NPN of this. We can take in the place of the PNP the equivalent of this and put it below but we have a β that will be the $\beta_1 \times \beta_2$ of two Darlington setups or using a pseudo-Darlington. So we put a pseudo-Darlington NPN transistor and the other will be of PNP type that appears here. So we can make mixtures in between. If we wish to have two output stages of NPN nature ie this transistor and this transistor the driver level towards the charge is the same, we can use instead of this transistor a Darlington setup of NPN Nature and a pseudo-Darlington instead of this transistor here, which makes the two transistors that see the charge the same.

Notes

Summary



Evolution du montage élémentaire



La forte augmentation du β réduit considérablement le courant de base

Electronique II

You can choose the same transistor that can guarantee a better match between the two levels.

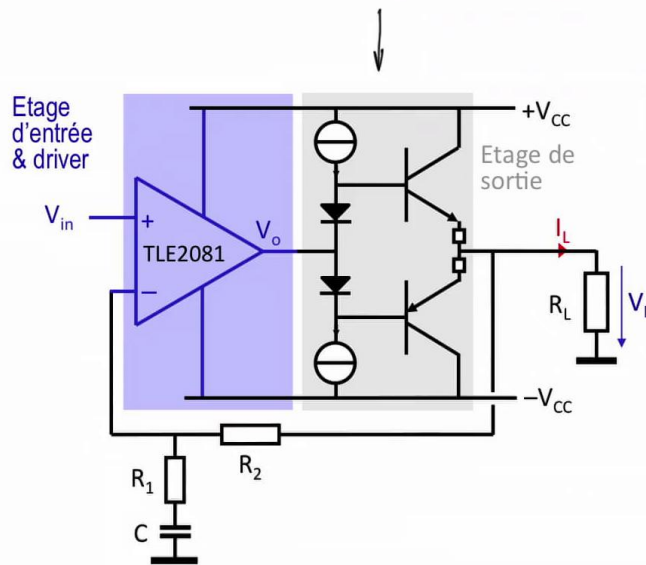
Notes

Summary

31m 17s



Amplificateur classe AB simple



$$P_L = \frac{\hat{V}_L \cdot \hat{I}_L}{2} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

$$P_{L, \text{max}, \text{théorique}} = \frac{V_{CC}^2}{2 \cdot R_L}$$

Exemple :

$$V_{CC} = 15 \text{ V} \quad R_L = 8 \text{ W}$$

$$P_{L, \text{max}, \text{théor.}} = 14 \text{ W}$$

$$V_{o, \text{max}} \approx \pm 12 \text{ V}$$

$$P_{L, \text{max}, \text{réelle}} \approx 9 \text{ W}$$

La limite fondamentale de la puissance de sortie du montage de base est liée à la tension d'alimentation et à la résistance de charge

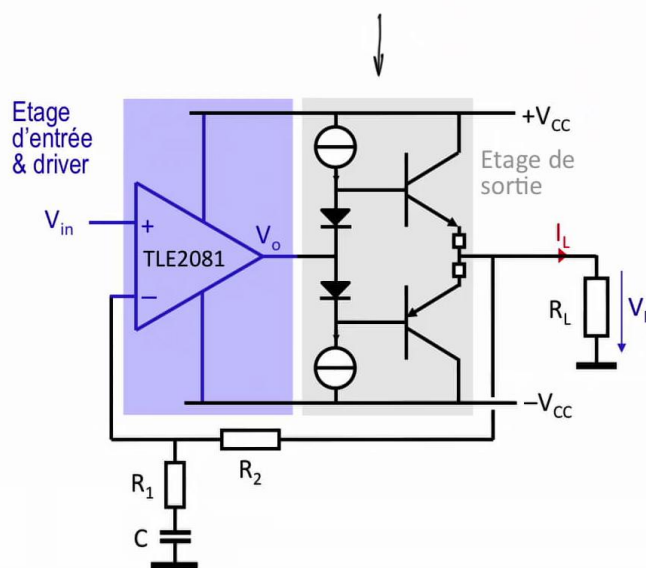
And finally, I'd like to give a very simple example on a simple class AB amplifier that anyone can go to a laboratory and plug. To do this, I have to make the diagram I have just presented, that is I have to take my output level and create a driver level that will control this level and that will allow me to make a counter reaction. So very often, or always the same, I will need an extra level that I will add to my amplifier which is a Class B or AB. So here in this case, I have a class AB power amplifier I added a market operational amplifier which on the inside contains a driver level that will get me the voltage, and contains a differential pair of input to be able to make a counter reaction from the outlet toward the inlet. So this is typical to the diagram that we make practically to make a low power amplifier. It is equivalent to something like this: if I take my scheme and I draw on the side that would give me this: I have a resistor.

Notes

Summary



Amplificateur classe AB simple



$$P_L = \frac{\hat{V}_L \cdot \hat{I}_L}{2} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

$$P_{L,max,theorique} = \frac{V_{CC}^2}{2 \cdot R_L}$$

Exemple :

$$V_{CC} = 15V \quad R_L = 8\Omega$$

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Electronique II

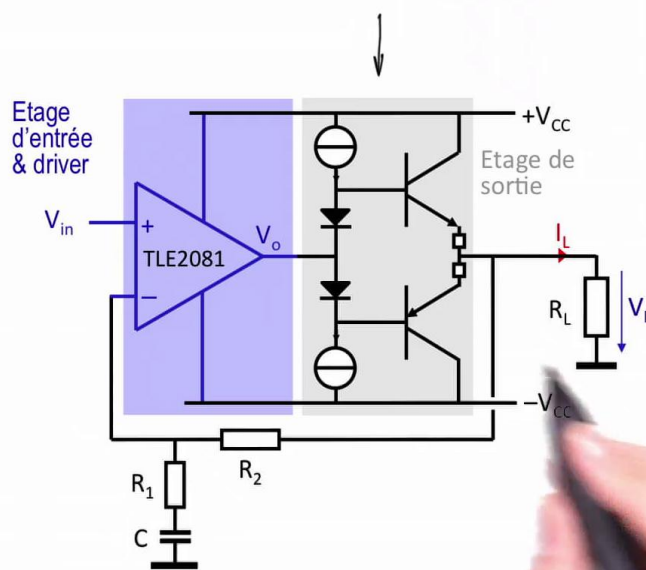
We'll take a loudspeaker because we will make an audio amp. I have a counter reaction with two resistors. This one, it is called R2. With a transfer function we will achieve a filter (inaudible) to avoid if ever there is an offset in my amp, this offset is not multiplied by the gain and returned. It is filtered by the capacitance here. When we have a trial voltage, this branch here will disappear, the capacitance is a short circuit. You hide it, you actually have a voltage follower a voltage follower which sees at the input the voltage you are going to put in on Vi. Very often in practice, it also makes a feed pass. (INAUDIBLE) up here on passive components to avoid also that there be a test component which is superimposed and appears in the speaker what we sought to avoid with this kind of amplifier. So I would take a loudspeaker 8 ohm for example. Unfortunately here there is a mistake. So I erase this. We will write the correct unit. I have a speaker of 8 ohm.

Notes

Summary



Amplificateur classe AB simple



$$P_L = \frac{\hat{V}_L \cdot \hat{I}_L}{2} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

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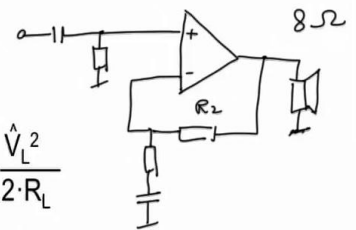
Exemple :

$$V_{CC} = 15 \text{ V} \quad R_L = 8 \, \Omega$$

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La limite fondamentale de la puissance de sortie du montage de base est liée à la tension d'alimentation et à la résistance de charge

Electronique II

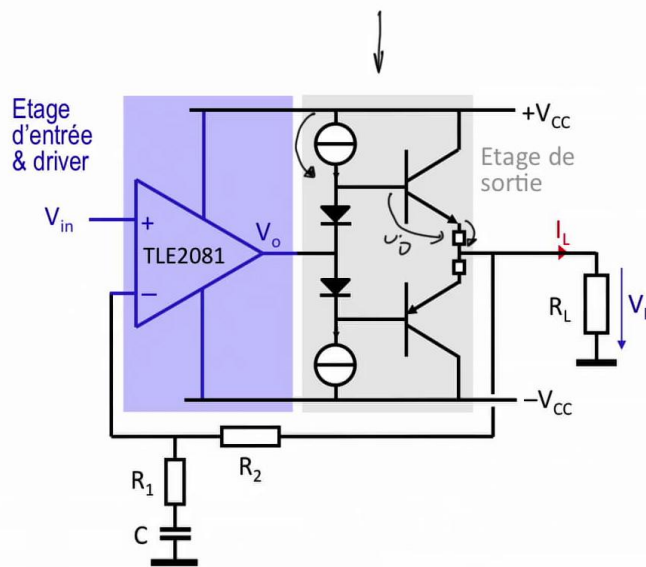
The first thing we do when you take a setup of this style, this is to evaluate the given power as we had said. Here in this example, I'll do a reverse engineering on the most I can get in power when I have a given supply voltage and I will establish it to roughly 15 volts. I purchased a component that is powered with about 15 volts and I will consider it as the $V_{CC} = 15 \text{ V}$ and -15 volts . And I have a speaker of $8 \, \Omega$. What is the maximum theoretical power? The maximum theoretical power it will tell you it is the $V_{CC} / 2 \times R_L$. So it will give me 14 watts. And you remember, we just said the output voltage may never reach V_{CC} . So here in this example, the theoretical power, I have considered that \hat{V}_i , the maximum value at the output is equal to V_{CC} . But actually, I have to subtract a small amount of a resistance that we add frequently in amplifiers when there is a level with bipolar because this resistance of a very, very low value about $0.2 \, \Omega$ prevents or limits the thermal runaway.

Notes

Summary



Amplificateur classe AB simple



$$P_L = \frac{\hat{V}_L \cdot \hat{I}_L}{2} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

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Electronique II

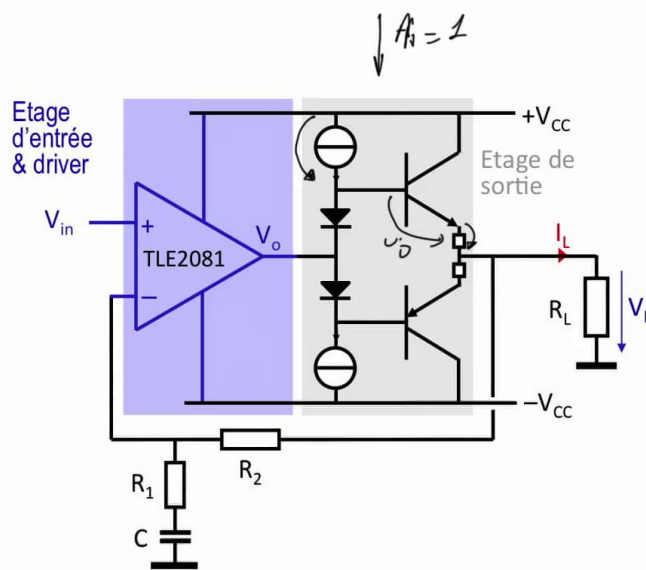
Now I have a voltage U_j . And then I have some component that I have to ensure before my current source saturates. So I have a voltage drop here, a voltage drop here, a voltage drop here that I must subtract from V_{CC} . So I can never reach this $V_{CC} = 15V$. So here, I took an example. Say assuming I have an increase of 4 volts and I reserve 3 volts for this path here, I'll end up with something correct in the order of ± 12 volts even with a 15 volt power supply. This brings me to a real max power about 9 watts. So that's one example. For someone who wants to make it in a laboratory by taking a market speaker and making an amplifier and taking an attack level and a counter reaction level in a simple amplifier embodying the counter reaction, could relatively easily plug this by keeping the power components on the outside. As this is a voltage follower you can always imagine that it is part of your amp.

Notes

Summary



Amplificateur classe AB simple



$$P_L = \frac{\hat{V}_L \cdot \hat{I}_L}{2} = \frac{\hat{V}_L^2}{2 \cdot R_L}$$

$$P_{L,max,theorique} = \frac{V_{CC}^2}{2 \cdot R_L}$$

Exemple :

$$V_{CC} = 15 \text{ V} \quad R_L = 8 \Omega$$

$$P_{L,max,theor.} = 14 \text{ W}$$

$$V_{o,max} \approx \pm 12 \text{ V}$$

$$P_{L,max,réelle} \approx 9 \text{ W}$$

La limite fondamentale de la puissance de sortie du montage de base est liée à la tension d'alimentation et à la résistance de charge

Electronique II

This tension and stress are the same, they follow. So this is a story that makes an A_v voltage gain which is equal to 1. So we have a voltage gain of 1. So if we can consider That this and this, it 's comparable in terms of gain calculation and it brings us to the real values of an embodiment of power if not higher than that. If someone will wish to make a complete amplifier by replacing this setup by a level of full transistors, he needs to make a gain level plus a differential pair. And that will be part of a detailed exercise that would be given after this video that summarizes, for those who realized it, an excellent summary of all of these courses you just followed throughout these videos because whoever happens to achieve the equivalent of a full setup for delivering power to the output, then he understood all the possible and imaginable uses of a transistor and the roles of the various setups that are in it. So I strongly urge you to do the exercise that will be given.

Notes

Summary



Conclusions



- La tension d'alimentation est adaptée à la puissance à fournir.
- L'étage driver est un ampli de classe A avec gain en tension élevé.
- L'étage d'entrée est généralement un ampli différentiel dont la sortie est adaptée à l'étage driver sélectionné.

Electronique II

To end this chapter on power amplifiers, I would just summarize what we just saw. So we analyzed the class A amplifier. We analyzed the class A, AB and B amplifiers. So with these three types of amplifiers, we can make audio amplifiers. I gave a little more focus on audio amplifiers. I'll give a complete exercise on the achievement of a class A amp and a class AB amplifier and it would be great for a student. What I would like to end with, for the two setups, it is often necessary to consider the supply voltages. So we understand that the power on the charge is done by the level of the supply voltage. Once we calculated the power we would like to have at the output based on the supply, we have a clear idea of the power value to set. Then in both cases, it is the voltage follower setups either A or AB. So we have an attack level and a counter a reaction level which should be achieved either by integrated elements either with components bought in the market which we realize with a large voltage gain and a differential level at the inlet to perform the counter reaction.

Notes

Summary



37m 25s